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Date 2/25/02 Serial # 09/892497 Priority Application Date 7/19/00

Your Name M. Lewis Examiner #

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In what format would you like your results? Paper is the default. PAPER DISK E-MAIL

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What is the topic, such as the novelty, motivation, utility, or other specific facets defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Novelty - pg 3 lines 22-27

Staff Use Only	Type of Search	Vendors
Searcher: [illegible]	Structure (#)	STN ✓
Searcher Phone: 306-6935	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation	Questel/Orbit
Date Searcher Picked Up: 3/11/02	Fulltext	Lexis-Nexis
Date Completed: 3/11/02	Patent Family	WWW/Internet
Searcher Prep/Rev Time: 130	Other	Other
Online Time: 90		

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SYSTEM:OS  - DIALOG OneSearch
  File 350:Derwent WPIX  1963-2001/UD,UM &UP=200216
         (c) 2002 Derwent Info Ltd
*File 350: Price changes as of 1/1/02. Please see HELP RATES 350.
More updates in 2002.  Please see HELP NEWS 350.
  File 347:JAPIO  Oct/1976-2001/Nov(Updated 020305)
         (c) 2002 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.


Set     Items   Description
S1       7672   HJFET OR HJFETS OR HBT OR HBTS OR HETERO()JUNCTION? OR HET-
             EROJUNCTION?
S2      34652   GAAS OR GALLIUM()MONOARSENIDE OR GALLIUM() ARSENIDE OR GA(-
             )AS
S3       3208   INGAAS OR IN(2W)GA(2W)AS
S4        192   GAASSB OR GA(2W)AS(2W)SB
S5         79   INGASB OR IN(2W)GA(2W)SB
S6      13228   INP OR IN()P OR INDIUM()PHOSPHIDE OR INDIUM()MONOPHOSPHIDE
S7        385   INASP OR IN(2W)AS(2W)P
S8        192   GAASSB OR GA(2W)AS(2W)SB
S9        142   INPSB OR IN(2W)P(2W)SB
S10      1015   SCHOTTKY(2N)CONTACT
S11     92567   (TRENCH?? OR HOLE? ? OR GROOVE? ? OR CHANNEL OR EDGE? ? OR
             FLUSH OR RIDGE?)(3N)(LAYER? OR FILM OR FILMS OR COAT????)
S12       120   (GRADED)(2N)( CHANNEL OR TRENCH?? OR HOLE? ? OR GROOVE? ? -
             OR CHANNEL OR EDGE? ? OR FLUSH OR RIDGE?)
S13      7334   BAND()GAP
S14     11622   SOURCE()ELECTRODE
S15     12003   DRAIN()ELECTRODE
S16      2183   S1 AND S2
S17       148   S16 AND S3
S18         1   S17 AND S12
S19        47   S17 AND S11
S20         1   S17 AND S12
S21        12   S19 AND (S14 OR S15)
S22        32   S17 AND GATE()ELECTRODE
S23         2   S22 AND S10
S24         6   S17 AND (S4 OR S5)
S25         5   S24 NOT (S18 OR S21)
S26        30   S17 AND S6
S27         6   S26 AND (S7:S9)
S28         2   S27 NOT (S18 OR S21 OR S24)
S29         0   S26 AND S12
S30         5   S26 AND S11
S31        19   S22 NOT (S18 OR S21 OR S24 OR S25 OR S27 OR S28 OR S30)
S32        18   S26 NOT (S18 OR S21 OR S24 OR S25 OR S27 OR S28 OR S30 OR -
             S22)
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? T S18/3,AB/1

18/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

02845670
SEMICONDUCTOR DEVICE

PUB. NO.: 01-143270 [JP 1143270 A]
PUBLISHED: June 05, 1989 (19890605)
INVENTOR(s): MATSUNO TOSHINOBU
INOUE KAORU
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-300708 [JP 87300708]
FILED: November 27, 1987 (19871127)
JOURNAL: Section: E, Section No. 815, Vol. 13, No. 396, Pg. 156, September 04, 1989 (19890904)

ABSTRACT
PURPOSE: To reduce the strain of a strain channel layer and the deterioration of electrical characteristics caused by the strain by varying the mixing ratio of a mixed crystal in a second mixed crystal semiconductor strain layer continuously from an interface between the strain layer and a first semiconductor layer, and making the ratio equal to that of a third semiconductor layer at an interface between the strain layer and the third semiconductor layer formed on the second multi-component mixed crystal semiconductor strain layer.

CONSTITUTION: The thickness of a **graded InGaAs** strain **channel** layer 6 is made 200 angstroms , and an In composition ratio at an interface between the layer 6 and a non-doped AlGaAs layer 5 formed on a substrate side is made 0.15. The ratio is continuously reduced toward a surface side, and the ratio is made 0 at an interface between the layer 6 and a non-doped **GaAs** layer 7 on the surface side so as to permit the layer 6 to change to **GaAs** without having any band gap. In a **hetero junction** between the **InGaAs** strain channel layer where two-dimensional electrons gather and the non- doped AlGaAs spacer layer 5, the In composition ratio is continuously reduced toward the surface side, keeping a band discontinuity gap .delta.Ec enough to form high concentration two-dimensional electron gas. And, the ratio is changed to that of **GaAs** at a hetero interface between the layer 6 and the non-doped **GaAs** layer 7, thereby gradually relieving the strain.

T S21/3,AB/1-4

21/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013905066
WPI Acc No: 2001-389279/200141
XRAM Acc No: C01-118663
XRPX Acc No: N01-286310

Heterojunction Field Effect Transistor (FET) having a large gate forward direction rising voltage

Patent Assignee: NEC CORP (NIDE); ANDO Y (ANDO-I); BITO Y (BITO-I)
Inventor: ANDO Y; BITO Y
Number of Countries: 030 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010005016	A1	20010628	US 2000739696	A	20001220	200141	B
JP 2001177089	A	20010629	JP 99361057	A	19991220	200141	
EP 1134810	A2	20010919	EP 2000127979	A	20001220	200155	

Abstract (Basic): US 20010005016 A1
Abstract (Basic):

NOVELTY - **Heterojunction** FET having a large gate forward direction rising voltage for use in mobile communication terminal.

DETAILED DESCRIPTION - The FET has an epitaxial structure comprising an undoped Al0.5Ga0.5As barrier layer having 3 - 10 nm thickness. The barrier layer is formed between an undoped In0.2Ga0.2As **channel layer** and a silicon doped Al0.2Ga0.8As upper electron supply layer, to form potential barrier just above a channel.

USE - Transistor for mobile communications.

ADVANTAGE - When a forward direction gate voltage is large, the gate current is reduced so that a gate forward direction rising voltage can be elevated. A large maximum drain current or a low on-resistance can be obtained.

DESCRIPTION OF DRAWING(S) - semi-insulative **GaAs** substrate

21/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012694216
WPI Acc No: 1999-500325/199942
XRAM Acc No: C99-146864
XRPX Acc No: N99-373483

Semiconductor device with **heterojunction** e.g. high speed mobility transistor - has undoped **gallium arsenide** buffer **layer**, undoped **channel** supply **layer**, undoped aluminium **gallium arsenide** spacer layer, silicon planar doped layer formed sequentially

Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11214676	A	19990806	JP 9810756	A	19980122	199942	B

Priority Applications (No Type Date): JP 9810756 A 19980122
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11214676	A		11	H01L-029/778	

Abstract (Basic): JP 11214676 A

NOVELTY - An undoped **GaAs** buffer layer (12), an undoped **InGaAs channel** supply **layer** (14), undoped AlGaAs spacer layer (16), an n-type AlGaAs carrier supply layer (18a), Si planar doped layer (28), n-type AlGaAs carrier supply layer (18b) and n- type **GaAs** cap layer (20) are formed sequentially on half-insulation **GaAs** substrate (10).

DETAILED DESCRIPTION - A recess (30) is formed such that a part of carrier supply layer (18a) is exposed and a gate electrode (26) is provided on the recess. The **source electrode** and **drain electrode** (24) connected by ohmic contact are provided on cap layer (20) on both sides of the recess.

21/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010830026
WPI Acc No: 1996-326978/199633
XRAM Acc No: C96-103747
XRPX Acc No: N96-275486

Hetero-junction-type field effect transistor mfg. method - involves removal of n-type **gallium arsenide** layer on p-type layer and contacting source-**drain electrode** with **channel layer**.

Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8148672	A	19960607	JP 94307073	A	19941117	199633	B

Priority Applications (No Type Date): JP 94307073 A 19941117
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8148672	A		6	H01L-029/778	

Abstract (Basic): JP 8148672 A

The mfg. method involves using a half insulation **GaAs** substrate (1) over which a convex shaped p-type **GaAs** layer (2) is formed. This p-type **GaAs** layer functions as a back gate layer. A non-doped **GaAs** buffer **layer** (3), an **InGaAs channel layer** (4), an n-type AlGaAs electro-supply layer (5) and an n-type **GaAs** layer (6) are formed sequentially over this back gate part and also on either side.

The n-type **GaAs** layer which acts as source-drain area is removed from the back gate part and a gate electrode (7) is formed over the electro-supply layer. SA **source electrode** (8) and a **drain electrode** (9) are formed on the n-type **GaAs** layer on either side of the back gate layer. Hence contact is made between source-**drain electrode** and the **channel layer**, without contacting the electronic supply layer.

21/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010697140
WPI Acc No: 1996-194095/199620
XRAM Acc No: C96-061544
XRPX Acc No: N96-162708
Hetero junction FET - includes i type indium-**gallium-arsenide channel layer** between undoped buffer **layer** and n type **channel layer**
Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8064807	A	19960308	JP 94200945	A	19940825	199620	B

Priority Applications (No Type Date): JP 94200945 A 19940825
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8064807	A		8	H01L-029/778	

Abstract (Basic): JP 8064807 A
The **hetero junction** FET consists of an undoped AlInAs buffer layer (2), an i type Iny Ga1-y As **channel layer** (3), an n type Inx Ga1-x As **channel layer** (30), and an undoped Al In As schottky type layer (5), which are formed sequentially on a semi insulated InP substrate (1). An n type **InGaAs** contact layer (6) and a gate electrode (9) are formed on the undoped AlInAs schottky type layer. A **source electrode** (7) and a **drain electrode** (8) are formed on the contact layer.

21/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010249299
WPI Acc No: 1995-150554/199520
XRAM Acc No: C95-069672
XRPX Acc No: N95-118261
Structure of **heterojunction** FET - uses silicon doped AlGaAs layer and Si doped **GaAs** layer to supply electrons
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7074347	A	19950317	JP 93171095	A	19930617	199520	B

Priority Applications (No Type Date): JP 93171095 A 19930617
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7074347	A		6	H01L-029/778	

Abstract (Basic): JP 7074347 A
The structure consists of a **GaAs** semiconductor substrate (1) on which a **GaAs** buffer layer (2), a non-doped AlGaAs layer (3) and first non-doped **InGaAs** layer (4) having a mixed crystal ratio of 0.2 In are formed. The film thickness of the non-doped **InGaAs** layer is about 150 Angstroms. Above this non-doped **InGaAs** layer a silicon doped **GaAs** layer (5) having a film thickness of 50 Angstroms and a doping density of 1x1018 cm-3 is formed. Over this, a silicon doped **GaAs** layer, a second non-doped **InGaAs** layer

(6) having a film thickness of 150 Angstroms and a mixed crystal ratio of 0.2 In is formed. Over this layer, a silicon doped AlGaAs layer (7) having a film thickness of 400 Angstroms and doping density of 1x1018cm-3 is formed. Then, silicon doped **GaAs** layer (8) is formed. Above these layers a gate electrode (9), **source electrode** (10) and **drain electrode** (11) are formed.
In the above mentioned layers, the silicon doped AlGaAs layer and silicon doped **GaAs** layer acts as electron supply layer. The first non-doped **InGaAs layer** acts as the **channel layer**.

21/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009317284
WPI Acc No: 1993-010748/199302
XRAM Acc No: C93-004839
XRPX Acc No: N93-008080
Heterojunction semiconductor device for microwave applications - having a reduced gate length and a novel **heterojunction** interface for transporting carriers with improved carrier mobility
Patent Assignee: FUJITSU LTD (FUIT)
Inventor: OHORI T
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 522943	A1	19930113	EP 92401928	A	19920703	199302	B
JP 5013461	A	19930122	JP 91162571	A	19910703	199308	
US 5326995	A	19940705	US 92907405	A	19920701	199426	

Abstract (Equivalent): EP 522943 B
A **heterojunction** semiconductor device comprising: a semi-insulating substrate (11) having an upper major surface; a **channel layer** (13) having upper and lower major surfaces and being provided above said upper major surface of said semi-insulating substrate for transporting carriers therethrough, said **channel layer** including a two-dimensional carrier gas (15a) formed therein along said upper major surface of said **channel layer**, the **channel layer** (13) comprising an undoped first sub-layer (14) of a first semiconductor material and an undoped second sub-layer (15) of a second semiconductor material, the first and second sub-layers having respectively first and second saturation drift velocities of carriers such that said first saturation drift velocity is substantially larger than said second saturation drift velocity; a carrier supplying layer (17) of a doped semiconductor material, said carrier supplying layer having upper and lower major surfaces and being provided above said upper major surface of said **channel layer**; **source electrode** means (21) provided above said upper major surface of said carrier supplying layer in ohmic contact therewith, for injecting carriers into said two-dimensional carrier gas via said carrier supplying layer; **drain electrode** means (22) provided above said upper major surface of said carrier supplying layer in ohmic contact therewith to be separated from said **source electrode** means, for recovering the carriers from said two-dimensional carrier gas via said carrier supplying layer; and gate electrode means (23) provided on said upper major surface of said carrier supplying layer between said source and **drain electrode** means for controlling a flow of the

carriers through said two-dimensional carrier gas; wherein: the first sub-layer (14) has a lower major surface, coincident with said lower major surface of said **channel layer** (13), and an upper major surface, and the second sub-layer (15) has an upper major surface coincident with said upper major surface of said **channel layer** and a lower major surface, said second sub-layer being provided on said first sub-layer, and the first and second sub-layers (14, 15) have first and second electron affinities respectively such that said second sub-layer (15) forms a potential well defined by a first potential barrier, which is formed in coincidence with said upper major surface of said second sub-layer (15), and a second, opposing potential barrier formed in coincidence with said lower major surface of said second sub-layer (15), said first and second potential barriers having first and second barrier heights respectively, wherein said first barrier height is substantially larger than said second barrier height.

21/3,AB/7 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06597537
FIELD-EFFECT TRANSISTOR

PUB. NO.: 2000-183334 [JP 2000183334 A]
PUBLISHED: June 30, 2000 (20000630)
INVENTOR(s): OKAMOTO YASUHIRO
APPLICANT(s): NEC CORP
APPL. NO.: 10-358338 [JP 98358338]
FILED: December 17, 1998 (19981217)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **heterojunction** field-effect transistor, where gm- characteristic is flattened, a distortion characteristic is improved and pinch-off property and top clogging can be dissolved satisfactorily.

SOLUTION: **GaAs**, a buffer layer 110 of AlGaAs, a lower electron supply layer 120 of n-type AlGaAs, a **channel layer** 130 of an i-type **InGaAs** , an upper electron supply layer 140 of n-type AlGaAs, a Schottky layer 150 of i-type AlGaAs, an ohmic contact layer 160A by n-type **GaAs** and the like, a gate electrode 170 of WSi, a **source electrode** 180 of Au, Ge and Ni, and a **drain electrode** 190 are formed on a **GaAs** semi-insulating substrate 100. Nt product of the upper electron supply layer 140 is set to about 1.4 times the maximum sheet carrier concentration Nsmax of a **heterojunction** interface and the Nt product of the lower electron supply layer 120 to about 1.1 times the maximum sheet carrier concentration Nsmax and to lie within the range of 1.0 times to 2.0 times.

21/3,AB/8 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05258059
P-TYPE FIELD-EFFECT SEMICONDUCTOR DEVICE, COMPLEMENTARY FIELD-EFFECT SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 08-213559 [JP 8213559 A]
PUBLISHED: August 20, 1996 (19960820)
INVENTOR(s): HARADA NAOKI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-016594 [JP 9516594]
FILED: February 03, 1995 (19950203)

ABSTRACT
PURPOSE: To provide a p-type field-effect semiconductor device which has high mobility of hole and lattice-matched with an InP substrate for easily obtaining a crystal of high quality to eliminate a lattice defect.

CONSTITUTION: The p-type field-effect semiconductor comprises a semi-insulating InP substrate 1, an InAlAs buffer layer 2, a **GaAs**(sub x)Sb(sub 1-x) **layer** (GaAsSb **channel layer** 3), a **hetero-junction** made of a second semiconductor layer (e.g. p-type InP **hole** supply **layer** 4) in which the upper end of a valance band is lower than that of the valence band of the **GaAs**(sub x)Sb(sub 1-x) layer, a p-type **InGaAs** contact layer 5, an Au-Zn-Au **source electrode** 6, an Au-Zn-Au **drain electrode** 7, and a Schottky electrode (Al gate electrode 8) formed on the front surface side from the second semiconductor layer. A voltage is applied to the Schottky electrode to vary the thickness of a depletion layer to thereby alter the two-dimensional hole gas concentration stored in the **GaAs** (sub x)Sb(sub 1-x) layer side of the **hetero junction**.

21/3,AB/9 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

05043267
FIELD-EFFECT TRANSISTOR

PUB. NO.: 07-335867 [JP 7335867 A]
PUBLISHED: December 22, 1995 (19951222)
INVENTOR(s): KUZUHARA MASAAKI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-123421 [JP 94123421]
FILED: June 06, 1994 (19940606)

ABSTRACT
PURPOSE: To provide a **hetero junction** field-effect transistor of two-step recess structure excellent in performance, uniformity and reproducibility, during the manufacture of which a selective etching technique is applied.

CONSTITUTION: On a semiinsulating **GaAs** substrate 1, the following are formed a buffer layer 2 made of undoped **GaAs** and undoped AlGaAs, an N-type AlGaAs electron supply layer 3, an undoped **InGaAs** **channel layer** 4, an AlGaAs electron supply layer 5 made of N-type AlGaAs and undoped AlGaAs, an N-type InGaP contact lower layer 16, and an N-type **GaAs** contact upper layer 7. A gate electrode is formed on the AlGaAs electron supply layer 5. A **source electrode** and a **drain electrode** are formed on the **GaAs** contact upper layer 7. The increase of drain current and the improvement of gate withstand voltage of a two-step recess structure FET can be attained.

21/3,AB/10 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

04519699
COMPOUND SEMICONDUCTOR **HETEROJUNCTION** FIELD-EFFECT TRANSISTOR

PUB. NO.:	06-163599 [JP 6163599 A]
PUBLISHED:	June 10, 1994 (19940610)
INVENTOR(s):	NEGISHI HITOSHI
APPLICANT(s):	NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.:	04-317008 [JP 92317008]
FILED:	November 26, 1992 (19921126)
JOURNAL:	Section: E, Section No. 1602, Vol. 18, No. 477, Pg. 140, September 06, 1994 (19940906)

ABSTRACT

PURPOSE: To reduce coulomb scattering of the interface between a spacer **layer** and a **channel layer** in a compound semiconductor **heterojunction** field-effect transistor and to improve the mutual conductance gm and noise figure by enhancing the electron mobility of two-dimensional electron gas.

CONSTITUTION: Undoped **GaAs** buffer layer 2, undoped **InGaAs** current **channel layer** 3, and N-type AlGaAs electron supply layer 5 are successively allowed to grow on a semi-insulation **GaAs** substrate 1. Then, a gate electrode 6, a **source electrode** 7, and a **drain electrode** 8 are formed.

21/3,AB/11 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

02777165
HETERO-JUNCTION FET

PUB. NO.:	01-074765 [JP 1074765 A]
PUBLISHED:	March 20, 1989 (19890320)
INVENTOR(s):	SUGIYAMA YOSHIHIRO
APPLICANT(s):	FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.:	62-233041 [JP 87233041]
FILED:	September 17, 1987 (19870917)
JOURNAL:	Section: E, Section No. 783, Vol. 13, No. 295, Pg. 72, July 07, 1989 (19890707)

ABSTRACT

PURPOSE: To prevent the deterioration of Schottky characteristics due to heating at the time of a process and heating in subsequent processes by using Si-doped InAlAs as a two-dimensional electron gas supply layer and Al as a gate electrode and inserting a **GaAs** layer between the two-dimensional electron gas supply layer and the gate electrode.

CONSTITUTION: Undoped InAlAs as a buffer layer 2, undoped **InGaAs** as a **channel layer** 3, undoped InAlAs as a spacer 4, and Si-doped N-InAlAs as an electron supply layer 5 are grown onto an InP substrate 1. Si-doped N-**GaAs** is grown onto the electron supply layer 5 as a diffusion preventive layer 6. Al is vacuum-deposited onto the layer 6, and a gate electrode is formed. Lastly, a **source electrode** 8 and a **drain electrode** 9 are shaped, and a surface inactivating film 10 is attached. An FET with a Schottky junction having the constitution displays excellent Schottky characteristics better than FETs with Schottky junctions having conventional structure in which no diffusion preventive layer 6 is formed.

21/3,AB/12 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

02656464
HETERO JUNCTION FIELD-EFFECT SEMICONDUCTOR DEVICE

PUB. NO.:	63-273364 [JP 63273364 A]
PUBLISHED:	November 10, 1988 (19881110)
INVENTOR(s):	ABE HITOSHI NISHI SEIJI
APPLICANT(s):	OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.:	62-106349 [JP 87106349]
FILED:	May 01, 1987 (19870501)
JOURNAL:	Section: E, Section No. 724, Vol. 13, No. 99, Pg. 73, March 08, 1989 (19890308)

ABSTRACT

PURPOSE: To obtain a semiconductor device having high 2-dimensional electron density by depositing a thin InAlAs film layer to become a carrier supply layer on a **GaAs** substrate while controlling a composition ratio and film thickness which do not cause a misfit dislocation due to a lattice mismatch, and forming an **InGaAs layer** to become a **channel layer** thereon while similarly controlling them.

CONSTITUTION: A non-doped GaAlAs layer 2 of approximately 1000 angstroms is grown by a molecular beam epitaxial method on a semi-insulating **GaAs** substrate 1 as a carrier supply layer. Then, a doped In(sub x1)Ga(sub 1-x1)As layer 3 of approximately 100 angstroms thick, a non-doped In(sub x1)Ga(sub 1-x1)As spacer layer 4 of approximately 40 angstroms thick and a non-doped In(sub y2)Ga(sub 1-y1)As layer 5 of approximately 100 angstroms are laminated and grown thereon as a **channel layer** of the degree that, when any of x1 and y2 are 0.2, the while thickness is approximately 250 angstroms . Then, a doped **GaAs** layer 6 is grown thereon, and a **source electrode** 7 and a **drain electrode** 8 between which a gate electrode 9 is interposed are mounted thereon.

T S23/3,AB/1-2

23/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06858169
FIELD-EFFECT SEMICONDUCTOR DEVICE

PUB. NO.: 2001-085671 [JP 2001085671 A]
PUBLISHED: March 30, 2001 (20010330)
INVENTOR(s): INAI MAKOTO
SASAKI HIDEHIKO
APPLICANT(s): MURATA MFG CO LTD
APPL. NO.: 11-256051 [JP 99256051]
FILED: September 09, 1999 (19990909)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **heterojunction** FET(field-effect transistor in **heterojunction** structure) that has a superior barrier function for a **gate electrode**, and at the same time a barrier layer with low series resistance for source and drain electrodes.

SOLUTION: On a semi-insulation **GaAs** substrate 42, a buffer layer 43, a non-doped **InGaAs** channel layer 44, a barrier layer 45 consisting of a plurality of layers, and a contact layer 46 that consists of n+ type **GaAs** and has a thickness of 50 nm are formed. The muti-layer barrier layer 45 has three-layer structure consisting of an n-type AlGaAs layer 45a, a non-doped AlGaAs layer 45b with a thickness of 2.5 to 5 nm, and an n-type AlGaAs layer 54c with a thickness of 10 nm. In a recess 47 where the contact layer 46 is partially eliminated, a **gate electrode** 50 is formed on an n-type AlGaAs layer 45c, and the bottom surface of the **gate electrode** 50 is buried to the n-type AlGaAs layer 45c for carrying out **Schottky contact** to the non-doped AlGaAs layer 45b.

23/3,AB/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03876329
FIELD EFFECT TRANSISTOR

PUB. NO.: 04-241429 [JP 4241429 A]
PUBLISHED: August 28, 1992 (19920828)
INVENTOR(s): NAKAJIMA SHIGERU
APPLICANT(s): SUMITOMO ELECTRIC IND LTD [000213] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-002790 [JP 912790]
FILED: January 14, 1991 (19910114)
JOURNAL: Section: E, Section No. 1303, Vol. 17, No. 9, Pg. 93, January 08, 1993 (19930108)

ABSTRACT

PURPOSE: To provide a high-output field effect transistor having an

excellent high-frequency characteristic.

CONSTITUTION: The first undoped semiconductor layer 23 and a channel layer 24 which is composed of In(sub y)Ga(sub 1-y)As (0<=Y<=0.35), has a crystal structure the lattice of which nearly matches that of the layer 23 and thin thickness, and contains an n-type impurity at a high concentration are successively formed on a **GaAs** semiconductor substrate 21. Then the second semiconductor layer 25 which has an excellent electron transporting characteristic and is composed of undoped **InGaAs** and the third semiconductor layer 26 composed of undoped Al(sub x)Ga(sub 1-x)As (0<=X<=0.3) are successively formed on the layer 24. The layer 26 forms a **heterojunction** together with the layer 25 and makes **Schottky contact** with a **gate electrode** 31.

T S25/3,AB/1-5

25/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013639127
WPI Acc No: 2001-123335/200113
XRAM Acc No: C01-035904
XRPX Acc No: N01-090539
Double **heterojunction** bipolar transistor fabrication includes forming a collector structure predominantly of indium phosphide, base and emitter
Patent Assignee: HRL LAB LLC (HRLH-N)
Inventor: DOCTOR D P; MATLOUBIAN M; MICOVIC M
Number of Countries: 093 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200109957	A1	20010208	WO 2000US20456	A	20000728	200113	B
AU 200063830	A	20010219	AU 200063830	A	20000728	200129	

A H01L-029/737 Based on patent WO 200109957

Abstract (Basic): WO 200109957 A1
Abstract (Basic):
NOVELTY - **Heterojunction** bipolar transistor formation comprises forming an InP collector; then a base structure, predominantly of **In**, **Ga**, **As** and **Sb**, then an emitter structure.
DETAILED DESCRIPTION - The proportions of the elements in the base structure are predominantly that in the quaternary compound InxGa1-xAsySb1-y in which x and y are selected so a
conduction band energy minimum of the quaternary compound is substantially aligned with a conduction band energy minimum of InP.
A region is defined between base and emitter edge farthest from the base, a delta doping step applied to form a layer. AN INDEPENDENT CLAIM is also included for the double **heterojunction** bipolar transistor device itself.

25/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013177742
WPI Acc No: 2000-349615/200030
XRAM Acc No: C00-106289
XRPX Acc No: N00-261927
Front-surface illuminated thermophotovoltaic device for energy conversion system has single crystal isolation layers, insulating member, ohmic contact, and spectral control device
Patent Assignee: US DEPT ENERGY (USAT)
Inventor: BALDASARO P F; CAMPBELL B C; CHARACHE G W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6057506	A	20000502	US 9878964	A	19980323	200030	B
			US 99275263	A	19990323		

Priority Applications (No Type Date): US 9878964 P 19980323; US 99275263 A 19990323
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6057506	A		11	H01L-035/04	Provisional application US 9878964

Abstract (Basic): US 6057506 A
Abstract (Basic):
NOVELTY - A front-surface illuminated thermophotovoltaic device (R) has a single crystal support substrate with isolation layers; single crystal thermophotovoltaic cells (8) on the isolation layers; an insulating member between cells; an ohmic contact for series cell connection; and a spectral control device (18) on top of the cells. Each cell has single crystal base and emitter layers.

25/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009685367
WPI Acc No: 1993-378921/199348
XRAM Acc No: C93-168197
XRPX Acc No: N93-292628
NPN **heterojunction** bipolar transistor with antimonide base - provides improved emitter injection efficiency, reduced power dissipation, and higher max. frequency of operation
Patent Assignee: HUGHES AIRCRAFT CO (HUGA)
Inventor: HASENBERG T C; STANCHINA W E
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 571994	A2	19931201	EP 93108534	A	19930527	199348	B
JP 6037104	A	19940210	JP 93127404	A	19930528	199411	
US 5349201	A	19940920	US 92889864	A	19920528	199437	

Abstract (Basic): EP 571994 A
An NPN-type **heterojunction** bipolar transistor (**HBT**) has (a) an emitter layer (18) including AlInAs or InP, (b) a base layer (16,32) including **Ga**, **As** and **Sb** and (v) a collector layer (14).
The substrate (12) comprises semi-insulating InP. In one embodiment, the base layer (16) lies between the emitter (18) and collector (14) layers, with the collector adjacent to the substrate. The collector layer is doped N-type and consists of **InGaAs**, InP or AlInAs. The base layer is doped P-type and consists of **GaAsSb**. In an alternative embodiment, the base layer comprises a strained layer superlattice (SLS) of alternate **GaAs** and GaSb layers, having 21-27 periods. The layers may be undoped, or one or both may be p-doped. The GaSb may be doped with Si and the **GaAs** with Be.
USE/ADVANTAGE - Used for high-speed electronic transistors of **HBT**-type. The use of Sb in the base layer, rather than In and As as in the prior art provides improved emitter injection efficiency, reduced power dissipation and higher max. frequency of oscillation (fmax.). Si can be used as a p-dopant which avoids the problems of using Be.

25/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008262417
WPI Acc No: 1990-149418/199020
XRAM Acc No: C90-065393
XRPX Acc No: N90-115819
Heterojunction semiconductor devices - with **heterojunction** between layers of indium **gallium arsenide** and indium aluminium arsenide, with electron gas at **heterojunction**
Patent Assignee: FUJITSU LTD (FUIT)
Inventor: ISHIKAWA T
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 368468	A	19900516	EP 89310136	A	19891004	199020	B
JP 2101751	A	19900413	JP 88252917	A	19881008	199021	
US 5023675	A	19910611	US 89416944	A	19891004	199126	
US 5118637	A	19920602	US 89416944	A	19891004	199225	
			US 91643375	A	19910122		

Abstract (Basic): EP 368468 A
Semiconductor device comprises: a substrate (11); first layer (12) of undoped **InGaAs**; second layer (13) of n-InAlAs forming a **heterojunction** (14); third layer (15) of n-**GaAsSb** with a groove (15a) through to the second layer contg. a gate electrode (16); and ohmic electrodes (17, 18) on the third layer. A two-dimensional electron gas is formed at the **heterojunction**. The substrate (11) is pref. InP; all the layers are lattice matched.
USE/ADVANTAGE - As a high-speed, high electron mobility transistor in which the gate is easily formed by etching.. (12pp Dwg.No.1/8
Abstract (Equivalent): EP 368468 B
A high electron mobility field effect transistor having a **heterojunction** and utilising a two-dimensional electron gas formed at said **heterojunction** comprising a substrate (11), a first semiconductor laser (12) of undoped indium **gallium arsenide** provided on said substrate, a second semiconductor layer (13) of n-type indium aluminium arsenide further provided on said first semiconductor layer so as to form said **heterojunction** between said first semiconductor layer, said second semiconductor layer having a top surface, a third semiconductor layer (15) of n-type **gallium arsenide** antimonide as a cap layer provided on the second semiconductor layer with a groove (15a) defined so as to expose region, a gate electrode (16) provided in alignment with said groove in contact with said exposed region of the second semiconductor layer, and ohmic electrodes (17,18) provided on the cap layer in ohmic contact therewith.

25/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

001659766
WPI Acc No: 1976-94228X/197650
Step graded ternary III-V **heterojunction** PN diode photodetector - using gallium indium arsenide of gallium arsenic antimonide alloys
Patent Assignee: BELL TEL LABS INC (AMTT); WESTERN ELECTRIC CO INC (AMTT)
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 3995303	A	19761130				197650	B

DE 2624348	A	19761215	197652
NL 7605855	A	19761206	197652

Abstract (Basic): US 3995303 A

A photodetector diode comprises (a) an n-type **GaAs** single cystal substrate, (b) a number of step-graded matching layers of **In-Ga-As** alloy on the substrate, with InAs increasing and n-type charge carrier concn. decreasing from the substrate, (c) a particular epitaxial layer of very lightly n-dope $In_xGa_{1-x}As$ on the last matching layer, where x is selected to make the band gap equal to the photo energy to be detected and the charge carrier conc. is <in any other semiconductor portion, (d) an epitaxial layer of p-type $In_yGa_{1-y}As$ on (c), where y is at least 0.02 <x, forming a window for photons and a pn **heterojunction** with (c), and (e) electrodes coupled to (c) and (d). admitting photons first to (d) then to (c). A similar structure has a p-type **GaAs** substrate and graded **GaAsSb** p-type layers, with Sb increasing and p-concn. decreasing from the substrate. A third embodiment comprises $GaAs_{1-x}Sb_x$ on a substrate and $GaAs_{1-y}Sb_y$ (x>y) forming a pn **heterojunction** with it. The diodes are useful detectors for wavelengths around 1.06 mu m. A pref. **InGaAs** diode has response over 0.9-09 mu m, 1.06 mu m peak, and a dark current within an order of magnitude of Si devices, while a pref. **GaAsSb** diode has a measured gain of 500.

28/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003215124
WPI Acc No: 1981-75681D/198141
Indium phosphide arsenide photovoltaic devices - have **heterojunction**(s) with indium tin oxide or indium **gallium arsenide**
Patent Assignee: BELL TELEPHONE LAB INC (AMTT)
Inventor: BACHMANN K J
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4291323	A	19810922				198141	B
JP 57001269	A	19820106	JP 8165313	A	19810501	198207	
JP 86050399	B	19861104				198648	

Priority Applications (No Type Date): US 80145610 A 19800501
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4291323	A		6		

Abstract (Basic): US 4291323 A
A device comprises a region of InAs(1-x)Px semiconductor; where x is greater than or equal to 0.85 and less than 1; in intimate contact with a second material, and an electrode for applying a voltage to the **InAsP**, pref. an Au/Zn alloy contact. In a first embodiment, the second material is In-Sn oxide or In oxide and a rectifying junction is formed; in a second, the second material is InyGa(1-y)As.
The devices are useful as photovoltaic or optoelectronic devices. With In(Sn) oxide, the devices exhibit unexpectedly high efficiencies, e.g. 15% for x = 0.95; with **InGaAs** the devices are useful for wavelengths over 1.65 micron and up to 1.85 micron.

28/3,AB/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05043388
COMPD. SEMICONDUCTOR DEVICE AND PRODUCTION PROCESS THEREOF

PUB. NO.: 07-335988 [JP 7335988 A]
PUBLISHED: December 22, 1995 (19951222)
INVENTOR(s): GOTO KATSUHIKO
TAKEMI MASAYOSHI
KINETSUKI HIROTAKA
MIHASHI YUTAKA
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-133088 [JP 94133088]
FILED: June 15, 1994 (19940615)

ABSTRACT
PURPOSE: To form an abrupt hetero-interface, relax the lattice mismatch, obtain the quantum effect enough and suppress the crystal from deteriorating, by adding Ga or Al to a converted layer formed by mixing As

in a barrier layer at the interface of a **heterojunction** of a well layer and barrier layer.
CONSTITUTION: After growing an Inlays quantum well layer 2 on an **InP** substrate 1, an **InP** barrier layer 3 is grown on the layer 2 and a Ga source is fed to form an **InGaAs** or InGaAsP eonverted layer 6. Among mixed crystals composed of **In**, **Ga**, **As** and **P**, InAs has the smallest band gap and high lattice constant. The barrier of the energy band of **InGaAs** formed by adding Ga grows high and the lattice deviation of its lattice constant decreases. Because of the dependence of the amount of remaining As on the feed rate of Ga and feed timing, this reduces the lowering of the barrier and lattice deviation due to forming of the layer 6.

30/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010697140
WPI Acc No: 1996-194095/199620
XRAM Acc No: C96-061544
XRPX Acc No: N96-162708
Hetero junction FET - includes i type indium-**gallium-arsenide channel layer** between undoped buffer **layer** and n type **channel layer**
Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8064807	A	19960308	JP 94200945	A	19940825	199620	B

Priority Applications (No Type Date): JP 94200945 A 19940825
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8064807	A		8	H01L-029/778	

Abstract (Basic): JP 8064807 A
The **hetero junction** FET consists of an undoped AlInAs buffer layer (2), an i type Iny Ga1-y As **channel layer** (3), an n type Inx Ga1-x As **channel layer** (30), and an undoped Al In As schottky type layer (5), which are formed sequentially on a semi insulated **InP** substrate (1). An n type **InGaAs** contact layer (6) and a gate electrode (9) are formed on the undoped AlInAs schottky type layer. A source electrode (7) and a drain electrode (8) are formed on the contact layer.
ADVANTAGE - Noise is suppressed during operation. High electron mobility and high speed operation are obtd. as well as high output.
Dwg.1/8

30/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009317284
WPI Acc No: 1993-010748/199302
XRAM Acc No: C93-004839
XRPX Acc No: N93-008080
Heterojunction semiconductor device for microwave applications - having a reduced gate length and a novel **heterojunction** interface for transporting carriers with improved carrier mobility
Patent Assignee: FUJITSU LTD (FUIT)
Inventor: OHORI T
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 522943	A1	19930113	EP 92401928	A	19920703	199302	B
JP 5013461	A	19930122	JP 91162571	A	19910703	199308	
US 5326995	A	19940705	US 92907405	A	19920701	199426	
EP 522943	B1	19961227	EP 92401928	A	19920703	199705	

Abstract (Equivalent): EP 522943 B
A **heterojunction** semiconductor device comprising: a

semi-insulating substrate (11) having an upper major surface; a **channel layer** (13) having upper and lower major surfaces and being provided above said upper major surface of said semi-insulating substrate for transporting carriers therethrough, said **channel layer** including a two-dimensional carrier gas (15a) formed therein along said upper major surface of said **channel layer**, the **channel layer** (13) comprising an undoped first sub-layer (14) of a first semiconductor material and an undoped second sub-layer (15) of a second semiconductor material, the first and second sub-layers having respectively first and second saturation drift velocities of carriers such that said first saturation drift velocity is substantially larger than said second saturation drift velocity; a carrier supplying layer (17) of a doped semiconductor material, said carrier supplying layer having upper and lower major surfaces and being provided above said upper major surface of said **channel layer**; source electrode means (21) provided above said upper major surface of said carrier supplying layer in ohmic contact therewith, for injecting carriers into said two-dimensional carrier gas via said carrier supplying layer; drain electrode means (22) provided above said upper major surface of said carrier supplying layer in ohmic contact therewith to be separated from said source electrode means, for recovering the carriers from said two-dimensional carrier gas via said carrier supplying layer; and gate electrode means (23) provided on said upper major surface of said carrier supplying layer between said source and drain electrode means for controlling a flow of the carriers through said two-dimensional carrier gas; wherein: the first sub-layer (14) has a lower major surface, coincident with said lower major surface of said **channel layer** (13), and an upper major surface, and the second sub-layer (15) has an upper major surface coincident with said upper major surface of said **channel layer** and a lower major surface, said second sub-layer being provided on said first sub-layer, and the first and second sub-layers (14, 15) have first and second electron affinities respectively such that said second sub-layer (15) forms a potential well defined by a first potential barrier, which is formed in coincidence with said upper major surface of said second sub-layer (15), and a second, opposing potential barrier formed in coincidence with said lower major surface of said second sub-layer (15), said first and second potential barriers having first and second barrier heights respectively, wherein said first barrier height is substantially larger than said second barrier height.

Dwg.4/7

Abstract (Equivalent): US 5326995 A

Heterojunction semiconductor device such as high electron mobility transistor has a semi-insulating **In P** substrate (11) on which a **channel layer** (14) of **In P** is gram epitaxially on a buffer layer (12) with further **In Ga As channel layer** (15), spacer **layer** (16) and n-type electron supplying layer (17) of In Al As. Ohmic electrodes (21,22) from source and drain electrodes. Schottky electrode (23) in channel region between these electrodes forms gate electrode.

ADVANTAGE - Maximises operational speed.

30/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008262417
WPI Acc No: 1990-149418/199020

XRAM Acc No: C90-065393
XRPX Acc No: N90-115819
Heterojunction semiconductor devices - with **heterojunction** between layers of indium **gallium arsenide** and indium aluminium arsenide, with electron gas at **heterojunction**
Patent Assignee: FUJITSU LTD (FUIT)
Inventor: ISHIKAWA T
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 368468	A	19900516	EP 89310136	A	19891004	199020	B
JP 2101751	A	19900413	JP 88252917	A	19881008	199021	
US 5023675	A	19910611	US 89416944	A	19891004	199126	
US 5118637	A	19920602	US 89416944	A	19891004	199225	
			US 91643375	A	19910122		

Abstract (Equivalent): EP 368468 B
A high electron mobility field effect transistor having a **heterojunction** and utilising a two-dimensional electron gas formed at said **heterojunction** comprising a substrate (11), a first semiconductor laser (12) of undoped indium **gallium arsenide** provided on said substrate, a second semiconductor layer (13) of n-type indium aluminium arsenide further provided on said first semiconductor layer so as to form said **heterojunction** between said first semiconductor layer, said second semiconductor layer having a top surface, a third semiconductor layer (15) of n-type **gallium arsenide** antimonide as a cap layer provided on the second semiconductor **layer** with a **groove** (15a) defined so as to expose region, a gate electrode (16) provided in alignment with said groove in contact with said exposed region of the second semiconductor layer, and ohmic electrodes (17,18) provided on the cap layer in ohmic contact therewith.

30/3,AB/4 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05258059
P-TYPE FIELD-EFFECT SEMICONDUCTOR DEVICE, COMPLEMENTARY FIELD-EFFECT SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 08-213559 [JP 8213559 A]
PUBLISHED: August 20, 1996 (19960820)
INVENTOR(s): HARADA NAOKI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-016594 [JP 9516594]
FILED: February 03, 1995 (19950203)

ABSTRACT
PURPOSE: To provide a p-type field-effect semiconductor device which has high mobility of hole and lattice-matched with an **InP** substrate for easily obtaining a crystal of high quality to eliminate a lattice defect.

CONSTITUTION: The p-type field-effect semiconductor comprises a semi-insulating **InP** substrate 1, an InAlAs buffer layer 2, a **GaAs**(sub x)Sb(sub 1-x) **layer** (GaAsSb **channel layer** 3), a **hetero-junction** made of a second semiconductor layer (e.g. p-type **InP hole** supply **layer** 4) in which the upper

end of a valance band is lower than that of the valence band of the **GaAs**(sub x)Sb(sub 1-x) layer, a p-type **InGaAs** contact layer 5, an Au-Zn-Au source electrode 6, an Au-Zn-Au drain electrode 7, and a Schottky electrode (Al gate electrode 8) formed on the front surface side from the second semiconductor layer. A voltage is applied to the Schottky electrode to vary the thickness of a depletion layer to thereby alter the two-dimensional hole gas concentration stored in the **GaAs** (sub x)Sb(sub 1-x) layer side of the **hetero junction**.

30/3,AB/5 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

02777165
HETERO-JUNCTION FET

PUB. NO.: 01-074765 [JP 1074765 A]
PUBLISHED: March 20, 1989 (19890320)
INVENTOR(s): SUGIYAMA YOSHIHIRO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-233041 [JP 87233041]
FILED: September 17, 1987 (19870917)
JOURNAL: Section: E, Section No. 783, Vol. 13, No. 295, Pg. 72, July 07, 1989 (19890707)

ABSTRACT

PURPOSE: To prevent the deterioration of Schottky characteristics due to heating at the time of a process and heating in subsequent processes by using Si-doped InAlAs as a two-dimensional electron gas supply layer and Al as a gate electrode and inserting a **GaAs** layer between the two-dimensional electron gas supply layer and the gate electrode.

CONSTITUTION: Undoped InAlAs as a buffer layer 2, undoped **InGaAs** as a **channel layer** 3, undoped InAlAs as a spacer 4, and Si-doped N-InAlAs as an electron supply layer 5 are grown onto an **InP** substrate 1. Si-doped N-**GaAs** is grown onto the electron supply layer 5 as a diffusion preventive layer 6. Al is vacuum-deposited onto the layer 6, and a gate electrode is formed. Lastly, a source electrode 8 and a drain electrode 9 are shaped, and a surface inactivating film 10 is attached. An FET with a Schottky junction having the constitution displays excellent Schottky characteristics better than FETs with Schottky junctions having conventional structure in which no diffusion preventive layer 6 is formed.

T S31/3,AB/1-19

31/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013700446
WPI Acc No: 2001-184670/200119
XRAM Acc No: C01-055567
XRPX Acc No: N01-131787
Element structure of **heterojunction** field effect transistor - embeds **gate electrode** over lower silicon doped **GaAs** layer, by penetrating upper silicon doped **GaAs** layer, thereby forming schottky junction
Patent Assignee: SHARP KK (SHAF)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11126898	A	19990511	JP 97292105	A	19971024	200119	B

Abstract (Basic): JP 11126898 A

NOVELTY - Si doped **GaAs** layers (8,9) with weaker electron affinity and large bandwidth, are formed over **InGaAs** buffer layers (6,7). Source-drain electrodes (10,11) are oppositely formed over the layer (9) with **gate electrode** (13) is embedded over layer (8) by penetrating layer (9), thereby forming the schottky junction.

DETAILED DESCRIPTION - **InGaAs** buffer layers (6,7) with smaller forbidden bandwidth and stronger electron affinity and a Si doped AlGaAs layer (5) are sequentially formed on a **GaAs** substrate (1).

USE - In **heterojunction InGaAs** FET.

ADVANTAGE - Stabilizes gate schottky characteristics by electron mobility and is used for high frequency power transistor.

DESCRIPTION OF DRAWING(S) - The figure shows sectional view of the FET. (1) **GaAs** substrate; (5) AlGaAs layer; (6,7) **InGaAs** buffer layers; (8,9) Si doped **GaAs** layers; (10) Source electrode; (11) Drain electrode; (13) **Gate electrode**.

31/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012675116
WPI Acc No: 1999-481223/199941
XRAM Acc No: C99-141746
XRPX Acc No: N99-358446
Group III-V semiconductor **heterojunction** field effect transistor
Patent Assignee: NEC CORP (NIDE); NIPPON ELECTRIC CO (NIDE)
Inventor: BITO Y; IWATA N
Number of Countries: 028 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 940855	A2	19990908	EP 99104470	A	19990305	199941	B
JP 11251575	A	19990917	JP 9854569	A	19980306	199949	
CN 1236998	A	19991201	CN 99103447	A	19990305	200015	

Abstract (Basic): EP 940855 A2

Abstract (Basic):
NOVELTY - A group III-V **heterojunction** field effect transistor has an electron accumulation layer on an undoped **GaAs** layer (112) giving high electron mobility, contact resistance from the cap to the channel layer is reduced and the ON resistance is low.
DETAILED DESCRIPTION - A field effect transistor comprises an undoped **InGaAs** or **GaAs** channel layer on which are sequentially an AlGaAs contact layer, a **GaAs** gate buried layer, an AlGaAs layer and a **GaAs** cap layer. A double recess is formed using the AlGaAs layers as etch stoppers (111), a third AlGaAs layer is heavily n-doped, a fourth **GaAs** layer includes an undoped layer (112) contacting the n-doped AlGaAs layer and a layer heavily n-doped and forming a top of the fourth **GaAs** layer, and the **GaAs** gate buried layer (110) and a **gate electrode** (114) contact each other directly.

31/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012238622
WPI Acc No: 1999-044730/199904
XRAM Acc No: C99-013999
XRPX Acc No: N99-032628
High electron mobility transistor - with heterostructure including indium **gallium arsenide** phosphide
Patent Assignee: LUCENT TECHNOLOGIES INC (LUCE)
Inventor: KUO J; WANG Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5844261	A	19981201	US 97868269	A	19970603	199904	B

Abstract (Basic): US 5844261 A
A transistor comprises a source and drain (12,14) and a heterostructure including a narrow bandgap channel (20.1) in which a quantum well is formed to confine electrons, with wider bandgap donor layers (20.2, 20.3) on either side of the channel for electron supply. A gate contact (30) applies voltage to control electron flow, the channel layers are of **InGaAs** and the donor layers of In0.5-q(AlxGa1-x)0.5+qP in which x = 0.2-0.3 and each donor layer forms a pseudomorphic **heterojunction** at the interface between them. The structure includes two pairs of spacer layers (20.4, 20.5, 20.6, 20.7) between the donor layers and the channel, each pair comprising an i-**GaAs** layer adjacent to the channel and an i-InAlGaP layer adjacent to a donor layer. Also claimed is a transistor as above in which the gate contact includes a **gate electrode** and a third wide bandgap layer forming a Schottky barrier.

31/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011836254
WPI Acc No: 1998-253164/199823
XRAM Acc No: C98-078928
XRPX Acc No: N98-199987
Field effect transistor - comprises **hetero-junction** semiconductor crystal and ohmic electrode

Patent Assignee: NEC CORP (NIDE); NIPPON ELECTRIC CO (NIDE); IWATA N (IWAT-I); YAMAGUCHI K (YAMA-I)
Inventor: IWATA N; YAMAGUCHI K; YAMAGUCHI Y
Number of Countries: 027 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 841691	A1	19980513	EP 97118738	A	19971028	199823	B
JP 10135242	A	19980522	JP 96288610	A	19961030	199831	
CA 2219598	A	19980430	CA 2219598	A	19971029	199836	
KR 98033346	A	19980725	KR 9756554	A	19971030	199932	
US 20010024846	A1	20010927	US 97958692	A	19971027	200159	
			US 2001862870	A	20010522		

Abstract (Basic): EP 841691 A

A field effect transistor (FET) comprises: (a) **hetero junction** semiconductor crystal having at least a channel layer of **InGaAs** or **GaAs**, a first layer of AlGaAs and a first layer of **GaAs**, a second layer of AlGaAs and an n-type second layer of **GaAs**; and (b) an ohmic electrode contacting the second **GaAs** layer and the channel layer, or, with the second **GaAs** layer and the first AlGaAs layer.

Also claimed are: (i) an FET as above in which the **hetero junction** crystal has a two stage recess structure removed from the first and second **GaAs** layers in stepwise fashion in the vicinity of the **gate electrode** forming portion; (ii) a FET as in (i) in which the n-type **GaAs** second layer is a high concentration layer; (iii) a FET as (i) in which the structure is channel layer of **InGaAs** or **GaAs**/AlGaAs/InAlAs or InAlGaAs/n-type **GaAs**, and the two stage recess is formed by removal of n-type **GaAs** and InAlAs or InAlGaAs in the vicinity of the **gate electrode**, whereby the **gate electrode** is formed on the AlGaAs layer and a gap is defined between it and the InAlAs or InAlGaAs layer so it does not make contact; (iv) the production of the FETs; and (v) a process as in (iv) in which the InAlAs or InAlGaAs is selectively etched on the AlGaAs layer using HCl:H2O = 1:x (where x < 6) and propagating the etch in the transverse direction by over-etching.

31/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011614631
WPI Acc No: 1998-031759/199803
Related WPI Acc No: 1996-238868
XRAM Acc No: C98-010685
XRPX Acc No: N98-025565
Method of forming N-type heterostructure insulated gate FET - uses two etch layers to form T-shaped gate with reduced leakage current and increased breakdown voltage
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: ABROKWAH J K; LUCERO R; ROLLMAN J A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5693544	A	19971202	US 95459855	A	19950602	199803	B
			US 96616293	A	19960315		

Abstract (Basic): US 5693544 A

A method of forming an N-type HIGFET (heterostructure insulated gate field effect transistor) comprises providing a III-V substrate (11) having a channel layer (12) that forms a **heterojunction** and includes a layer of **InGaAs** on which is a **GaAs** protective layer. An insulator containing more than 50%Al (16) is formed on the substrate, followed by two etch-stop layers (17,18) and a doped **GaAs** layer (19) on which a **gate electrode** is formed (21). The gate is undercut by removing part of the doped **GaAs** layer and exposed second etch layer and first etch layer are removed. Using the gate as a mask dopant is formed in the substrate so that the dopant edge is a given distance from the insulator edge.

Also claimed is a **GaAs** HIGFET as above using a **GaAs** substrate, intrinsic **GaAs** on the insulator, intrinsic AlAs on this and a doped **GaAs** layer before forming the gate as above.

31/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011127813
WPI Acc No: 1997-105737/199710
XRAM Acc No: C97-033835
XRPX Acc No: N97-087540

Mfg. FET with **heterojunction** structure - involves embedding **gate electrode** on N-aluminium **gallium arsenide** electronic feed layer, through second recess opening of indium gallium phosphide ohmic contact layer

Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8340012	A	19961224	JP 95168337	A	19950609	199710	B

Priority Applications (No Type Date): JP 95168337 A 19950609
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8340012	A		4	H01L-021/338	

Abstract (Basic): JP 8340012 A

The mfg method involves forming an N-AlGaAs electronic feed layer (2) on an undoped **InGaAs** or **GaAs** channel layer (1). An InGaP and n+ type **GaAs** ohmic contact layers (3,4) are sequentially formed on the electronic feed layer. A first recess opening is formed, by etching highly the n+ type **GaAs** contact layer. A second recess opening is formed, by etching the InGaP contact layer.

The width of the first recess opening is greater than the second recess opening. A **gate electrode** (7) is formed on the feed layer through the second recess opening. Source-drain electrodes (5,6) are formed on the exposed surfaces of the n+ type **GaAs** contact layer.

ADVANTAGE - Improves product yield. Offers high frequency power. Obtains large output.

Dwg.1/2

31/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009933838
WPI Acc No: 1994-201550/199425
XRPX Acc No: N94-158557
Heterojunction two-dimensional electron gas FET with increased conduction band discontinuity - has **heterojunction** formed between undoped indium **gallium arsenide** channel layer and uniformly silicon doped indium aluminium gallium phosphide n-type electron supply layer
Patent Assignee: NEC CORP (NIDE)
Inventor: KUZUHARA M; MARUHASHI K; ONDA K
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 602671	A2	19940622	EP 93120429	A	19931217	199425	B
JP 6188271	A	19940708	JP 92337287	A	19921217	199432	
US 5466955	A	19951114	US 93167407	A	19931214	199551	
			US 95380251	A	19950130		

Abstract (Basic): EP 602671 A
The FET includes a semi-insulating substrate (21) with an undoped buffer layer (23) on the substrate surface (22). There is an n-type doped InAlGaP semiconductor layer (25) on an undoped **InGaAs** layer (24) on the buffer layer, forming a **heterojunction** structure. The substrate is pref. **GaAs**, with pref. a 200nm thick **GaAs** buffer layer. The **InGaAs** layer acts as a channel layer and pref. has a thickness of 15nm. The InAlGaP layer acts as an electron supply layer and pref. is 30nm thick and uniformly doped with silicon at an impurity density of 2x1018/cm3.
The transistor is completed by a **gate electrode** (29) on the electron supply layer and two ohmic electrodes (27,28) on a 60nm thick n-type doped **GaAs** cap layer (26). The conduction band discontinuity, measured between the channel and electron supply layers, is 0.41eV.

31/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008828690
WPI Acc No: 1991-332707/199145
XRAM Acc No: C91-143702
XRPX Acc No: N91-255015
Complementary **heterojunction** field effect transistor - with aniso-type N-gate for P-channel devices giving improved gate leakage and speed and power characteristics
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: ABROKWAH J K; HUANG J H; WU S Y
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5060031	A	19911022	US 90584014	A	19900918	199145	B
JP 4245650	A	19920902	JP 91254147	A	19910906	199242	

Abstract (Basic): US 5060031 A
A complementary **GaAs** based heterostructure IC structure comprises sequential layers, on a **GaAs** substrate major surface, of an epitaxial layer of substantially intrinsic **GaAs**; an epitaxial layer of substantially intrinsic AlGaAs; an epitaxially grown layer of substantially intrinsic **GaAs**; an epitaxial layer of

substantially intrinsic **InGaAs**; an epitaxial layer of substantially intrinsic AlAs; a substantially intrinsic AlGaAs layer. First and second N-type regions are formed in the surface of the AlGaAs layer and extend to the third (**GaAs**) layer, wherein a portion of the **InGaAs** layer which lies between the 2 N-type regions forms a channel of an N-channel HFET.

The structure further comprises a conductive material formed on top of the AlGaAs layer, between and sepd. from the N-type regions, and making a rectifying contact with the AlGaAs layer, serving as a **gate electrode** of the N-channel HFET; source-drain electrodes of the N-channel HFET formed on the N-type regions; first and second P-type regions formed in the surface of AlGaAs and extending to the second **GaAs** layer, so that a portion of the **InGaAs** layer which lies between the P-type regions forms a channel of a P-channel HFET; an epitaxially grown N-type an isotype region covering a portion of the AlGaAs layer between and sepd. from the P-type regions; an epitaxially grown pre-ohmic layer covering the N-type an isotype region; a conductive material formed on top of the pre-ohmic layer and making contact with it, to serve as a **gate electrode** of the P-channel HFET; electrodes formed on the P-type regions to serve as source-drain electrodes of the P-channel HFET; an insulating region formed between the N-channel and the P-channel HFET.

31/3,AB/9 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06858170
FIELD-EFFECT SEMICONDUCTOR DEVICE

PUB. NO.: 2001-085672 [JP 2001085672 A]
PUBLISHED: March 30, 2001 (20010330)
INVENTOR(s): INAI MAKOTO
SASAKI HIDEHIKO
APPLICANT(s): MURATA MFG CO LTD
APPL. NO.: 11-256059 [JP 99256059]
FILED: September 09, 1999 (19990909)

ABSTRACT
PROBLEM TO BE SOLVED: To reduce series resistance passing through the semiconductor layer between contact and channel layers where an ohmic electrode is provided a in a **heterojunction** FET(field effect transistor in **heterojunction** structure).

SOLUTION: On a semi-insulation **GaAs** substrate 42, a buffer layer 43, an n-type **InGaAs** channel layer 44, a multilayer barrier layer 45 (an n-type AlGaAs layer 45a, a non-doped AlGaAs layer 45b, and an n-type AlGaAs layer 45c), and an n+ type **GaAs** contact layer 46 are formed. A **gate electrode** 50 is buried into the n-type AlGaAs layer 45c in a recess 47 where the contact layer 46 is partially removed. In this case, the barrier and contact layers 45 and 46, and the channel and barrier layers 44 and 45 are in iso-type **heterojunction**.

31/3,AB/10 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06858169
FIELD-EFFECT SEMICONDUCTOR DEVICE

PUB. NO.: 2001-085671 [JP 2001085671 A]
PUBLISHED: March 30, 2001 (20010330)
INVENTOR(s): INAI MAKOTO
SASAKI HIDEHIKO
APPLICANT(s): MURATA MFG CO LTD
APPL. NO.: 11-256051 [JP 99256051]
FILED: September 09, 1999 (19990909)

ABSTRACT
PROBLEM TO BE SOLVED: To provide a **heterojunction** FET(field-effect transistor in **heterojunction** structure) that has a superior barrier function for a **gate electrode**, and at the same time a barrier layer with low series resistance for source and drain electrodes.

SOLUTION: On a semi-insulation **GaAs** substrate 42, a buffer layer 43, a non-doped **InGaAs** channel layer 44, a barrier layer 45 consisting of a plurality of layers, and a contact layer 46 that consists of n+ type **GaAs** and has a thickness of 50 nm are formed. The muti-layer barrier

layer 45 has three-layer structure consisting of an n-type AlGaAs layer 45a, a non-doped AlGaAs layer 45b with a thickness of 2.5 to 5 nm, and an n-type AlGaAs layer 54c with a thickness of 10 nm. In a recess 47 where the contact layer 46 is partially eliminated, a **gate electrode** 50 is formed on an n-type AlGaAs layer 45c, and the bottom surface of the **gate electrode** 50 is buried to the n-type AlGaAs layer 45c for carrying out Schottky contact to the non-doped AlGaAs layer 45b.

31/3,AB/11 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06185348
SEMICONDUCTOR DEVICE

PUB. NO.: 11-126898 [JP 11126898 A]
PUBLISHED: May 11, 1999 (19990511)
INVENTOR(s): SHIODA MASAHIRO
APPLICANT(s): SHARP CORP
APPL. NO.: 09-292105 [JP 97292105]
FILED: October 24, 1997 (19971024)

ABSTRACT
PROBLEM TO BE SOLVED: To provide the semiconductor device of a high electron mobility for power, for which Schottky junction characteristics are stabilized.

SOLUTION: A first semiconductor layer doped with (n)-type impurities, a second semiconductor layer formed on the first semiconductor layer whose electron affinity is stronger and whose forbidden bandwidth is smaller than that of the first semiconductor layer and whose third semiconductor layer doped with the (n)-type impurities whose electron affinity is weaker and forbidden band width is larger than the second semiconductor layer are laminated on a **GaAs** substrate 1 in this order. Then this semiconductor device is provided with a source electrode 10 and a drain electrode 11 facing opposite the third semiconductor layer by an ohmic junction and a **gate electrode** 13 facing the third semiconductor layer by a Schottky junction. The third semiconductor layer which is **GaAs** doped with the (n)-type impurities, the second semiconductor layer is **InGaAs** and a **heterojunction** field effect transistor the electron density of which is 3×1012 cm-2 obtained.

31/3,AB/12 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

05193172
HETERO JUNCTION TYPE OF FIELD EFFECT TRANSISTOR, AND ITS MANUFACTURE

PUB. NO.: 08-148672 [JP 8148672 A]
PUBLISHED: June 07, 1996 (19960607)
INVENTOR(s): NIWA SHIGEKI

APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-307073 [JP 94307073]
FILED: November 17, 1994 (19941117)

ABSTRACT
PURPOSE: To reduce the source resistance without increasing gate leak, and control the threshold voltage without providing a back gate.

CONSTITUTION: A p-type **GaAs** layer (back gate layer) 2 in the shape of a projection is made on a semiinsulating **GaAs** substrate 1 ((a)). A nondoped **GaAs** layer 3 to serve as a buffer layer, an **InGaAs** layer 4 to serve as a channel layer, an n-type AlGaAs layer 5 to serve as an electron supply layer, and an n-type **GaAs** layer 6 to serve as a source and drain region are grown in order ((b)-(d)). The n-type **GaAs** layer 6 on the p-type **GaAs** layer 2 is removed, and a **gate electrode** 7, and source and drain electrodes 8 and 9 are made ((e)).

31/3,AB/13 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

05019821
FIELD EFFECT TRANSISTOR AND ITS MANUFACTURE

PUB. NO.: 07-312421 [JP 7312421 A]
PUBLISHED: November 28, 1995 (19951128)
INVENTOR(s): FUJIWARA AKIRA
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-101469 [JP 94101469]
FILED: May 17, 1994 (19940517)

ABSTRACT
PURPOSE: To prevent the deterioration of element characteristics due to oxidation of an InAlAs layer, by forming a **GaAs** layer which is formed on an InAlAs layer and is thinner than or equal to a critical film thickness and a **gate electrode** which controls the electron concentration of an electron storing layer in the **InGaAs** layer and is composed of metal having a melting point higher than or equal to a specific temperature.

CONSTITUTION: On a semiinsulative InP substrate 11 the following are formed; an In(sub x)Ga(sub 1-x)As (0<x<1.0) layer 13, an In(sub y)Al(sub 1-y)As (0<y<1.0) layer 14 forming a **heterojunction** with discontinuity of a specific conduction band to form an electron storing layer in the layer 13, a **GaAs** layer 15 which is in contact with the In(sub y)A(sub 1-y)As layer 14 and thinner than or equal to the critical film wherein dislocation due to lattice unconformity is generated, and a **gate electrode** 19 wherein metal having a melting point of 1600 deg.C or higher is arranged in the part in contact with the layer 15. Thereby oxidation of the InAlAs layer 14 and reaction of the **gate electrode** 19 and the **GaAs** layer 15 are restrained, so that the thermal stability of an element can be improved.

31/3,AB/14 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

04725508
P-CHANNEL **HETEROJUNCTION** FIELD-EFFECT TRANSISTOR

PUB. NO.: 06-196508 [JP 6196508 A]
PUBLISHED: July 15, 1994 (19940715)
INVENTOR(s): HIKOSAKA YASUMI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-344761 [JP 92344761]
FILED: December 24, 1992 (19921224)

ABSTRACT
PURPOSE: To increase the current supply capability per unit gate width and the level of integration, by forming a hole supply layer by utilizing the energy level in a quantum well layer and applying high concentration doping to a narrow region.

CONSTITUTION: On a **GaAs** substrate 1 the following are formed in order; an I-**GaAs** buffer layer 2, an I-**InGaAs** channel layer 3, an I-InGaP quantum well barrier layer 4, a **GaAs** quantum well layer 5, a hole supply layer 6, I-InGaP quantum well barrier layer 7, an I-AlGaAs layer 8, a **gate electrode** 9 of Al or the like, and source/drain electrodes of AuZn/Au or the lile. As compared with the conventional HEMT, the hole concentration can be increased without generating the limitation of the supply amount of carrier concentration, and the hole mobility can be improved without enlarging the gate width. Thereby a complementary element excellent in the N and P balance can be realized.

31/3,AB/15 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

03880548
FIELD EFFECT TRANSISTOR

PUB. NO.: 04-245648 [JP 4245648 A]
PUBLISHED: September 02, 1992 (19920902)
INVENTOR(s): NAKAJIMA SHIGERU
HAYASHI HIDEKI
APPLICANT(s): SUMITOMO ELECTRIC IND LTD [000213] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-010880 [JP 9110880]
FILED: January 31, 1991 (19910131)
JOURNAL: Section: E, Section No. 1305, Vol. 17, No. 15, Pg. 82, January 12, 1993 (19930112)

ABSTRACT
PURPOSE: To obtain a high output FET excellent in high frequency characteristics.

CONSTITUTION: On a **GaAs** semiconductor substrate 21, the following are formed in order; a semiconductor layer 22 composed of undoped **GaAs**, a first semiconductor layer 23 composed of undoped **InGaAs**, a first channel layer 24 composed of high concentration thin-layered N(sup +) type **InGaAs**, a second semiconductor layer 25 composed of undoped **InGaAs** , a second channel layer 26 similar to the first channel layer

24, and a third semiconductor layer 27 composed of undoped **InGaAs**. Further on the third semiconductor layer 27, a fourth semiconductor layer 28 composed of undoped Al(sub x)Ga(sub 1-x)As is formed. The fourth semiconductor layer 28 forms a **hetero junction** together with the third semiconductor layer 27, and is in Shottky contact with a **gate electrode** 33.

31/3,AB/16 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

03876329
FIELD EFFECT TRANSISTOR

PUB. NO.: 04-241429 [JP 4241429 A]
PUBLISHED: August 28, 1992 (19920828)
INVENTOR(s): NAKAJIMA SHIGERU
APPLICANT(s): SUMITOMO ELECTRIC IND LTD [000213] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-002790 [JP 912790]
FILED: January 14, 1991 (19910114)
JOURNAL: Section: E, Section No. 1303, Vol. 17, No. 9, Pg. 93, January 08, 1993 (19930108)

ABSTRACT

PURPOSE: To provide a high-output field effect transistor having an excellent high-frequency characteristic.

CONSTITUTION: The first undoped semiconductor layer 23 and a channel layer 24 which is composed of In(sub y)Ga(sub 1-y)As (0<=Y<=0.35), has a crystal structure the lattice of which nearly matches that of the layer 23 and thin thickness, and contains an n-type impurity at a high concentration are successively formed on a **GaAs** semiconductor substrate 21. Then the second semiconductor layer 25 which has an excellent electron transporting characteristic and is composed of undoped **InGaAs** and the third semiconductor layer 26 composed of undoped Al(sub x)Ga(sub 1-x)As (0<=X<=0.3) are successively formed on the layer 24. The layer 26 forms a **heterojunction** together with the layer 25 and makes Schottky contact with a **gate electrode** 31.

31/3,AB/17 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

03407245
HETERO JUNCTION FIELD EFFECT TRANSISTOR AND MANUFACTURE THEREOF

PUB. NO.: 03-070145 [JP 3070145 A]
PUBLISHED: March 26, 1991 (19910326)
INVENTOR(s): MATSUMOTO FUMIO
NAKANO HARUO
APPLICANT(s): SANYO ELECTRIC CO LTD [000188] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-207613 [JP 89207613]
FILED: August 09, 1989 (19890809)
JOURNAL: Section: E, Section No. 1077, Vol. 15, No. 233, Pg. 95, June 14, 1991 (19910614)

ABSTRACT

PURPOSE: To obtain a stable ohmic electrode of low resistance and excellent Schottky characteristics by arranging a specified electron supply layer of high impurity concentration in the position closer to a semi-insulating substrate than a specified channel layer and arranging a non-doped or low-impurity-concentration barrier layer in the position near a surface, and electrodes on said barrier layer.

CONSTITUTION: On an electron supply layer 3 formed on a semi-insulating substrate 1, a channel layer 5 and a barrier layer 6 are laminated in order in this constitution. Compared with the forbidden band width of the channel layer 5, that of the electron supply layer and of the barrier layer are made wider. The electron supply layer 3 is composed of Al(sub x)Ga(sub 1-x)As or In(sub x)'Al(sub 1-x)'As, and the channel layer 5 is composed of In(sub y)Ga(sub 1-y)As, further the barrier layer 6 is composed of **GaAs**. As the electron supply layer 5 composed of AlGaAs is located in the position closer to the substrate 1 than the channel layer composed of **InGaAs** , even if an Si concentration in the electron supply layer is made higher, influence of the **gate electrode** upon Schottky characteristics is little. Also, as a non-doped or low-Si-concentration **GaAs** layer is located closer to a surface than the channel layer, it can realize the stability of an ohmic electrode, elimination of a **hetero junction** barrier resistance, reduction of resistors connected to sources in series, and enhancement of a gate withstanding voltage.

31/3,AB/18 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

02611863
SEMICONDUCTOR DEVICE

PUB. NO.: 63-228763 [JP 63228763 A]
PUBLISHED: September 22, 1988 (19880922)
INVENTOR(s): OHORI TATSUYA
TAKIGAWA MASAHIKO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-063026 [JP 8763026]
FILED: March 18, 1987 (19870318)
JOURNAL: Section: E, Section No. 706, Vol. 13, No. 26, Pg. 59, January 20, 1989 (19890120)

ABSTRACT

PURPOSE: To improve the performance of a high electron-mobility FET by forming the **hetero-junction** of an **InGaAs** layer and an InGaP layer, to which an impurity is doped, and using the **InGaAs** layer as the channel of interface- quantized carriers.

CONSTITUTION: An AlGaAs buffer layer 2, an **InGaAs** layer 3, an InGaP electron supply layer 4 and a **GaAs** layer 5 are shaped onto a semi-insulating **GaAs** substrate 1. Source-drain electrodes 8 are patterned onto the layer by employing AuGe/Au, etc., and alloy regions 8A are formed in depth reaching the layer 3 through heat treatment. A **gate electrode** 9 is shaped onto the layer 5. According to such constitution, the surface concentration of a two-dimensional electron gas

is increased by the **hetero-junction** of the layer 3 and the layer 4. Since the electrode 9 is formed onto the layer 5, the large height of a Schottky barrier is acquired, thus improving performance.

31/3,AB/19 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

01863268
FIELD EFFECT TRANSISTOR

PUB. NO.: 61-077368 [JP 61077368 A]
PUBLISHED: April 19, 1986 (19860419)
INVENTOR(s): TOKUDA HIROKUNI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-198570 [JP 84198570]
FILED: September 25, 1984 (19840925)
JOURNAL: Section: E, Section No. 431, Vol. 10, No. 248, Pg. 85, August 26, 1986 (19860826)

ABSTRACT
PURPOSE: To obtain the title element whose operating layer is an **InGaAs** layer having the good microwave characteristic of small gate leakage current and small resistance, by providing an **InGaAs** layer in high electron density and an InP layer in low electron density, and the former is made as the main current path.

CONSTITUTION: The electron density of the **InGaAs** layer 2 in lattice matching with a semi-insulation InP substrate 101 is 2X10(sup 17)cm-(sup 3), and that of the InP layer 3 is 1X10(sup 14)cm(sup -3). Further, a **gate electrode** 4g forming the Schottky junction with the InP layer 2 is made of gold. Next, a source electrode 4s and a drain electrode 4 make ohmic contacts with the **InGaAs** layer 2 each, and is made of AuGe/Ni. This layer 2 itself is used as the electron transit region 5. The operation principle of this element is basically equal to that of the present **GaAs** MESFET except that the gate has the **hetero junction** of **InGaAs**/InP.

? T S32/3,AB/1-18

32/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014276086
WPI Acc No: 2002-096788/200213
XRAM Acc No: C02-030031
XRPX Acc No: N02-071477
Fabrication of submicron gate by selectively anisotropic etching dummy emitter at region where line is defined, and depositing contact metal on etched portion of dummy emitter
Patent Assignee: HANKOOK KAGAKU GIJUTSUIN (KOKA-N); KIM M J (KIMM-I); KWON Y S (KWON-I); YANG K H (YANG-I)
Inventor: KIM M J; KWON Y S; YANG K H
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010026985	A1	20011004	US 2000749785	A	20001228	200213	B
JP 2001284365	A	20011012	JP 2000374444	A	20001208	200213	

Abstract (Basic): US 20010026985 A1
Abstract (Basic):
NOVELTY - A submicron gate is fabricated by selectively anisotropic etching a dummy emitter at a region where a line is defined, to allow the dummy emitter to have an etched portion having a bottom surface with a width less than the width of the line defined by a photoresist; and depositing a contact metal on the etched portion of the dummy emitter, thus forming a gate.
DETAILED DESCRIPTION - Fabrication of a submicron gate includes:
(a) laminating a dummy emitter defining a dummy emitter region over a **heterojunction** bipolar transistor structure including layers sequentially formed over a semiconductor substrate (11) to define a base region (16), an emitter region, and an emitter cap region, respectively;
(b) defining a line having a width of about 1 mum on the dummy emitter by use of a photoresist while using a contact aligner;
(c) selectively anisotropic etching the dummy emitter at a region where the line is defined, to allow the dummy emitter to have an etched portion having a bottom surface with a width less than the width of the line defined by the photoresist; and
(d) depositing a contact metal (91) on the etched portion of the dummy emitter, thus forming a gate.

32/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013845548
WPI Acc No: 2001-329761/200135
XRPX Acc No: N01-237339
Metamorphic **heterojunction** bipolar transistor for high power transistor amplifier has heavily doped n type **InGaAs** layer which represents ohmic contact for emitter
Patent Assignee: CHAO P (CHAO-I); LIN T Y (LINT-I); WU C (WUCC-I); WIN SEMICONDUCTORS CORP (WINS-N); CHAO P S (CHAO-I); LIN T Y C (LINT-I); WU C S (WUCS-I); WENMAO SEMICONDUCTOR CO LTD (WENM-N)

Inventor: CHAO P; LIN T Y; WU C; CHAO P S; LIN T Y C; WU C S
Number of Countries: 007 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 10049148	A1	20010419	DE 1049148	A	20001004	200135	B
CA 2322080	A1	20010407	CA 2322080	A	20001003	200135	
FR 2799884	A1	20010420	FR 200012813	A	20001006	200135	
JP 2001144101	A	20010525	JP 2000292682	A	20000926	200136	

Abstract (Basic): DE 10049148 A1
Abstract (Basic):
NOVELTY - A heavily doped n type **InGaAs** layer (26) represents an ohmic contact for an emitter represented by a n type InAlAs layer or a graded n type AlInGaAs layer or a n type **InP** layer (25). A heavily doped p type layer (24) represents a base and an ohmic contact or the base. A heavily doped n type **InGaAs** layer (22) represents an ohmic contact for a collector.
DETAILED DESCRIPTION - The collector is represented by a n type **InGaAs** layer or a n type **InP** layer or a n type InAlAs layer (23). A non doped metamorphic buffer layer (21), the heavily doped n type **InGaAs** layer, the n type InAlAs layer, the heavily doped p type layer, the n type **InP** layer, and the heavily doped n type **InGaAs** layer are sequentially laminated on a semiconducting **GaAs** substrate (20).

32/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013736955
WPI Acc No: 2001-221185/200123
XRAM Acc No: C01-066569
XRPX Acc No: N01-157711
Group III-V semiconductor device, e.g. **heterojunction** bipolar transistor, has electrode with reaction area in N-type or I-type compound semiconductor layer due to solid phase reaction of platinum layer with semiconductor layer
Patent Assignee: TERATECH INC (TERA-N)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001023994	A	20010126	JP 99191908	A	19990706	200123	B

Abstract (Basic): JP 2001023994 A
Abstract (Basic):
NOVELTY - P-type **GaAs** or **InGaAs** compound semiconductor layer (1) is laminated on N-type or I-type compound semiconductor layer (2) containing InGaP, InAlGaAs, InAlAs, AlGaAs or **InP**. Electrode structure is comprised by reaction area (4) formed in N-type or I-type compound semiconductor area, Pt layer (3) and the electrode (5) where reaction area is comprised by solid phase reaction of the Pt with the layer (2).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for compound semiconductor device manufacturing method.
USE - In **heterojunction** bipolar transistor (**HBT**) with specific electrode structure.

32/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012644231
WPI Acc No: 1999-450336/199938
XRPX Acc No: N99-336817
Heterojunction type hot electron transistor - has base layer having lattice constant different from lattice constants of collector and emitter, to cause Fermi level transition in conduction band or valence band
Patent Assignee: NIPPON TELEGRAPH & TELEPHONE CORP (NITE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11186539	A	19990709	JP 97356811	A	19971225	199938	B

Priority Applications (No Type Date): JP 97356811 A 19971225
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11186539	A		7	H01L-029/68	

Abstract (Basic): JP 11186539 A

NOVELTY - The base layer (B) is made of InAs or **GaAs** whose lattice constant is different from that of emitter and collector layers (E,C). When the base layer is configured between emitter and collector layers to form a **heterojunction**, transition in Fermi level of conduction band or valence band is caused due to mismatching of lattice constants. DETAILED DESCRIPTION - The emitter and the collector layers of the transistor are comprised of **GaAs**, AlAs, **InP** or **InGaAs** crystals. The energy band gap of base layer is smaller than that of collector layer and the emitter layer.

USE - **Heterojunction** type hot electron transistor.

ADVANTAGE - As the lattice constant of base layer different from that of emitter and collector layers, causes Fermi level transition, effect of electron scattering, impurity scattering are reduced and **heterojunction** of good quality is formed, thereby by making high speed operation of transistor possible. DESCRIPTION OF DRAWING(S) - The figure shows the energy band diagram of **heterojunction** type hot electron transistor. (B) Base layer; (C) Collector layer; (E) Emitter layer.

32/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012433280
WPI Acc No: 1999-239388/199920
XRAM Acc No: C99-070273
XRPX Acc No: N99-178654
Semiconductor lamination structure for **heterojunction** bipolar photo-transistor - has N-type **indium phosphide** emitter layer and indium **gallium arsenide** layer formed sequentially on substrate
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11068141	A	19990309	JP 97224123	A	19970820	199920	B

Priority Applications (No Type Date): JP 97224123 A 19970820

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11068141	A		6	H01L-031/10	

Abstract (Basic): JP 11068141 A

NOVELTY - An **indium phosphide** layer (11) is formed on insulated indium phosphorus substrate (10). A N-type indium **gallium arsenide** layer (12) is formed on the indium phosphorus layer.

DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is included for manufacture of semiconductor lamination device.

USE - For **heterojunction** bipolar photo-transistor.

ADVANTAGE - Keeps indium phosphorus layer surface plane by performing **InGaAs** layer on **InP** continuously. Reduces contact resistance by etching emitter layer, using indium **gallium arsenide** emitter contact layer as mask.

32/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009382257
WPI Acc No: 1993-075735/199309
Related WPI Acc No: 1992-064500
XRPX Acc No: N93-058261

Compound semiconductor FET bipolar darlington pair mfr. method for e.g. mm wave multistage amplifier - having p-channel MISFET and NPN **HBT** combined in n-type **indium phosphide** active region on semi-insulating substrate

Patent Assignee: ALLIED-SIGNAL INC (ALLC)
Inventor: AINA O A; MARTIN E A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5187110	A	19930216	US 90593459	A	19901005	199309	B
			US 91792104	A	19911113		

Abstract (Basic): US 5187110 A

The method involves forming a semi-insulating **InP** substrate having an n-type **InP** active region from any suitable group III-V compound semi-conductor combining a p-channel MISFET and an NPN **HBT** on the semi-insulating substrate and electrically isolating the p-channel MISFET and NPN **HBT** by implanting isolation regions in the active region.

A p+type **InGaAs** layer is formed above the active region with overlaid n-type **InP** and SiO_2 layers. A TiAu layer over the SiO_2 layer providing a terminal for Vin, an AuGeNi layer over the active region, providing a terminal for ground and an AuGeNi layer over the n-type **InP** layer, providing a terminal for Vcc are formed in sequence. Pref. the active region is formed by ion implantation followed by annealing and the step of forming the active region is by epitaxial growth.

32/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008968976
WPI Acc No: 1992-096245/199212

XRAM Acc No: C92-044645
XRPX Acc No: N92-072046
Refractory metal ohmic contacts formation on III-V semiconductors - gives low-resistance self-aligned contacts using the same mask for ion-implantation and metallisation
Patent Assignee: NORTHROP CORP (NOTH)
Inventor: TULLY J W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5093280	A	19920303	US 89385027	A	19890725	199212	B

Abstract (Basic): US 5093280 A

Forming a refractory metal ohmic contact on a gp.III-V semiconductor substrate (12) comprises forming an implant-metallisation mask (26) having at least one window on it, implanting Zn, Be, Cd or Mg ions through the window to form a p region, depositing a refractory metal (W, Mo or Ta) through the window to form a contact with the doped substrate, and then thermally activating this to give the refractory ohmic contact of specific contact resistance of less than 10 power (-6) ohm-cm2.

Also claimed is a method where the refractory metal is deposited through the mask prior to the implantation stepurther claimed is a method in which the substrate is **GaAs**, the mask includes at least a silica layer and metal deposition is either before or after ion implantation.

Pref. the refractory is Mo or Mo followed by Cr layers. Pref. a passivation layer, pref. Cr followed by Si3N4 is deposited over the Mo before activation. Pref. Mo is deposited by vapour deposition and passivation is by vapour deposition of Cr and sputtering of nitride. Pref. the substrate is **GaAs**, GaP, GaSb, InAs, **InP**, InSb or lattice-matched heterosystems contg. these elements and Al, pref. GaAlAs or **InGaAs**.

32/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008584561
WPI Acc No: 1991-088593/199113
XRAM Acc No: C91-037624
XRPX Acc No: N91-068499
Semiconductor body comprising a mesa - mfd. using wet etch and anodic oxidn. to produce mesa with a flat side wall
Patent Assignee: PHILIPS ELECTRONICS NV (PHIG); PHILIPS GLOEILAMPENFAB NV (PHIG); KONINK PHILIPS ELECTRONICS NV (PHIG); US PHILIPS CORP (PHIG)
Inventor: BINSMA J J M; TIJBURG R P
Number of Countries: 008 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 418953	A	19910327	EP 90202404	A	19900910	199113	B
NL 8902292	A	19910402	NL 892292	A	19890914	199117	
JP 3106026	A	19910502	JP 90242278	A	19900912	199124	
US 5266518	A	19931130	US 90576317	A	19900829	199349	

Abstract (Equivalent): US 5266518 A
Semiconductor body comprising a mesa is mfd. from two layers of different semiconductors, the first being thinner than the second, are provided. A mask is formed on the second layer, which is etched with a wet etchant, with no underetching beneath the mask. Part of the second layer is converted into oxide by non-selection anodic oxidn. and is removed by an etchant selective between the layers, so that the second layer is underetched. The first layer is etched to form a mesa. Pref. substrate is In phosphide, first layer is **In Ga As** or **In Ga As** phosphide, and second layer is In phosphide.

32/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008512364
WPI Acc No: 1991-016448/199103
XRAM Acc No: C91-007057
XRPX Acc No: N91-012693
Heterojunction bipolar transistor for large scale prodn. - is easily mfd. and permits high density on ics
Patent Assignee: AMERICAN TELEPHONE & TELEGRAPH CO (AMTT); AT & T BELL LAB (AMTT)
Inventor: LUNARDI L M; MALIK R J; RYAN R W
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 408252	A	19910116	EP 90307351	A	19900705	199103	B
US 5001534	A	19910319	US 89378534	A	19890711	199114	

Abstract (Equivalent): US 5106766 A
Semiconductor device (I) is made that comprises p-type III-V semiconductor material (II). (II) is grown by exposing a substrate to at least a first and a second molecular or atomic species, these species comprising a column III and a column V chemical element, respectively.

The method also comprises heating a graphite body such that the growing (II) is exposed to sublimated C-atoms, and C-atoms are incorporated into (II).

Pref. (I) is an n-p-n **heterojunction** bipolar transistor. Pref. (II) comprises Ga and As. Pref the substrate is exposed to a flux of the first and second atomic species in a growth chamber.

ADVANTAGE - Device so obtd. can have high current gain with very small emitter stripe width, and can be readily made.

US 5001534 A

The bipolar transistor has (a) an emitter region of 1st semiconductor material 5-25 nm thick overlying the base region and such that the portion overlying the extrinsic base region is fully depleted of conduction dectors at all bias voltages within the normal operation of the transistor, and (b) means to make electrical contact to the base region comprising an ohmic contact. The emitter stripe width associated with the base region is about 1 micron. The layer of 1st material serves as a base passivation layer and is doped AlGaAs, AlGaSb, **InP**, InAlAs, GaAsP, Si, GaP, **GaAs** or CdTe, and the base region is doped **GaAs**, **InGaAs**, AlGaAs, GaSb, SiGe, Si, Ge or HgTe.

32/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004471054
WPI Acc No: 1985-297932/198548
XRPX Acc No: N85-221810

Integrated **heterojunction** FET and photodiode for fibre optics - substrate transparent to wavelength of infrared radiation used for optical communications to cause current to flow through diode

Patent Assignee: INT STANDARD ELECTRIC CORP (INTT)
Inventor: GHOSH C L; PHATAK S B
Number of Countries: 006 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 162541	A	19851127				198548	B
JP 60233855	A	19851120	JP 8564942	A	19850328	198602	

Abstract (Basic): EP 162541 A

A substrate of semi-insulating **InP** material has a layer of n-type **InGaAs** provided on one of its major surfaces. Formations (3,4) of a p-type material, especially **InGaAs** or **InP**, are provided on the n-type **InGaAs** for the diode and transistor. Contact metallisation (5,6) are provided on the top of both types of formations and source and drain electrodes (7,8) are provided on the n-type **InGaAs** layer on opposite sides of the transistor formation.

A diode contact is arranged on the n-type **InGaAs** layer next to the diode formation. The substrate is transparent to a particular wavelength of infrared radiation so that light directed at the against the diode region through the substrate causes current flow through the diode.

32/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

002561693
WPI Acc No: 1980-79718C/198045

Semiconductor layer mfr. - by vapour phase formation of **indium phosphide** layer on indium **gallium arsenide** layer deposited by liquid epitaxial growth method
Patent Assignee: NIPPON TELEGRAPH & TELEPHONE CORP (NITE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 55123126	A	19800922				198045	B

Priority Applications (No Type Date): JP 7929387 A 19790315

Abstract (Basic): JP 55123126 A
In P semiconductor layer is deposited by means of vapour growth technique on **InGaAs** semiconductor layer deposited by liquid epitaxial growth technique.
In P substrate is contacted to **In** melt containing **Ga** and **As** to deposit **InGaAs** layer thereon. For depositing **InP** layer on **InGaAs** layer by using vapour growth techniques, HCl is contacted to In to produce a chloride of In, and the In chloride is carried with H2 gas and the gas is mixed with PH3. The mixed gas is carried on **InGaAs** layer and contacted thereto to deposit **InP** layer thereon. These epitaxial growth processes are carried out simultaneously by using a reaction chamber.
The **InP** layer is formed on **InGaAs** layer without melting **InGaAs** layer and semiconductor light sources, such as laser devices, with double **heterojunctions** are easily manufactured by the proposed method.

32/3,AB/12 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06916564
MODIFIED **HETEROJUNCTION** BIPOLAR TRANSISTOR

PUB. NO.: 2001-144101 [JP 2001144101 A]
PUBLISHED: May 25, 2001 (20010525)
INVENTOR(s): CHAO PENG-SHENG
WU CHAN-SHIN
LIN YEN-CHIN
APPLICANT(s): WIN SEMICONDUCTORS CORP
APPL. NO.: 2000-292682 [JP 2000292682]
FILED: September 26, 2000 (20000926)
PRIORITY: 99 158026 [US 99158026], US (United States of America), October 07, 1999 (19991007)

ABSTRACT
PROBLEM TO BE SOLVED: To provide a modified **heterojunction** bipolar transistor having a structure for material with high efficiency and low-voltage operability.

SOLUTION: This modified **heterojunction** bipolar transistor has a semi-insulating **Ga As** substrate, undoped modified barrier film, and a heavily-doped n-type **InGaAs** film, forming an ohmic electrode of a collector in response with the structure of material for a **GaAs** wafer. Therefore, the modified **heterojunction** bipolar transistor includes a lightly-doped n-type **InGaAs** or **InP** or InAlAs film, forming a collector of the modified **heterojunction** bipolar transistor, heavily-doped n-type **InGaAs** film forming a base of the

modified **heterojunction** bipolar transistor for an ohmic base electrode, an n-type **InGaAs** or inclined AlInGaAs or **InP** film forming an emitter of the modified **heterojunction** bipolar transistor, and the heavily-doped **InGaAs** film forming an ohmic emitter electrode of the modified **heterojunction** bipolar transistor.

32/3,AB/13 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06179913
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 11-121462 [JP 11121462 A]
PUBLISHED: April 30, 1999 (19990430)
INVENTOR(s): SHIGEMATSU HISAO
APPLICANT(s): FUJITSU LTD
APPL. NO.: 09-275854 [JP 97275854]
FILED: October 08, 1997 (19971008)

ABSTRACT

PROBLEM TO BE SOLVED: To form a surface protection film of an **InP/ InGaAs hetero junction** bipolar transistor with good reproducibility, by using a lamination film consisting of an **InP** layer and an InGaAsP layer as a surface protection film.

SOLUTION: A lamination film consisting of an **InP** layer 4 and an InGaAsP layer 5 is used as a surface protection film and a guard ring for an **InP/InGaAs hetero junction** bipolar transistor(**HBT**). As a result, it is possible to eliminate the need for etching the **InP** layer 4 to remain thin and to form a surface protection film of a uniform thickness without increasing manufacturing processes. If the InGaAsP layer 5 is provided between the **InP** layer 4 which becomes an emitter layer and an **InGaAs** emitter cap layer 7, the InGaAsP layer 5 becomes an etching stopper layer, and it is possible to obtain small energy discontinuous level ΔEc at a conduction band side formed in **InP /InGaAs** interface and to reduce a resistance of **InP/GaAs** interface.

32/3,AB/14 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

05332797
HETEROJUNCITON BIPOLAR TRANSISTOR AND ITS MANUFACTURE

PUB. NO.: 08-288297 [JP 8288297 A]
PUBLISHED: November 01, 1996 (19961101)
INVENTOR(s): YAMAHATA SHIYOUJI
MATSUOKA YUTAKA
APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-087944 [JP 9587944]

FILED: April 13, 1995 (19950413)

ABSTRACT

PURPOSE: To provide good reproducibility in composition controllability during the deposition of mixed crystal layer and to restrict a periphery base leak current by forming a stair-shaped guard ring construction circumscribed to an emitter layer having uniform band gap energy.

CONSTITUTION: An emitter layer 5 comprising a semiconductor having a band gap larger than that of a base layer 4 and an emitter contact layer 6 comprising a semiconductor having a band gap smaller than that of a base layer 4 are provided. The emitter layer has AlGaAs of a constant composition in AlGaAs/ **GaAs**-based **heterojunction** bipolar transistor (**HBT**), and the emitter layer 5 has **InP** in an **InP/InGaAs** -based type. A step-shaped emitter guard ring construction 8 is provided for the peripheral length portion of an emitter/base junction circumscribed to the emitter layer 5 with a constant band gap in the thickness direction. By doing this, a base leak current can be restricted in the emitter mesa peripheral portion even though **HBT** dimension is made finer.

32/3,AB/15 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

04980525
FABRICATION OF SEMICONDUCTOR DEVICE

PUB. NO.: 07-273125 [JP 7273125 A]
PUBLISHED: October 20, 1995 (19951020)
INVENTOR(s): SHIGEMATSU HISAO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-058444 [JP 9458444]
FILED: March 29, 1994 (19940329)

ABSTRACT

PURPOSE: To provide means for forming a surface protective layer accurately and uniformly on a base layer through a simple process.

CONSTITUTION: A transition layer 3 of InGaAsP is inserted between an emitter layer 4 of **InP** in an **InP/InGaAs** based **HBT** and a base layer 2 of **InGaAs**. The transition layer 3 serves as an etching stopper at the time of etching the emitter layer 4 thus forming a surface protective layer of accurate thickness. A transition layer having double layer structure of an InGaP layer and an InGaAsP layer is inserted between an emitter layer of **GaAs** and a base layer of **GaAs**. The transition layer 3 serves as an etching stopper at the time of etching the emitter layer 4 and realizes an ideal band alignment thus lowering the implantation energy.

32/3,AB/16 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

04183428
MANUFACTURE OF HIGH IMPURITY CONCENTRATION SEMICONDUCTOR LAYER

PUB. NO.: 05-175128 [JP 5175128 A]
PUBLISHED: July 13, 1993 (19930713)
INVENTOR(s): ANAYAMA CHIKASHI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-303115 [JP 91303115]
FILED: November 19, 1991 (19911119)
JOURNAL: Section: E, Section No. 1451, Vol. 17, No. 579, Pg. 74, October 21, 1993 (19931021)

ABSTRACT

PURPOSE: To simply grow a high impurity concentration semiconductor layer by using MOVPE method effective for mass production in the manufacture of the high impurity concentration semiconductor layer.

CONSTITUTION: When an organometal vapor-phase epitaxy method and a temperature with low limits, where no hillock is generated, concretely a temperature not exceeding 500 deg.C are applied, it is made possible to grow III/V compound semiconductor layer containing a high concentration impurity, e.g. Zn, for determining a conductive type, e.g. **InGaAs** layer lattice-matching with **InP** substrate or **InGaAs** layer lattice-matching with **GaAs** substrate or **GaAs** layer. Further, all various compound semiconductor crystal layers used in presently used compound semiconductor devices, e.g. semiconductor laser, photodiode, **HBT**, etc., can be formed by the application of the organometal vapor-phase epitaxy method.

32/3,AB/17 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

03345440
HETERO JUNCTION BIPOLAR TRANSISTOR

PUB. NO.: 03-008340 [JP 3008340 A]
PUBLISHED: January 16, 1991 (19910116)
INVENTOR(s): KATO RIICHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-034405 [JP 8934405]
FILED: February 14, 1989 (19890214)
JOURNAL: Section: E, Section No. 1048, Vol. 15, No. 118, Pg. 151, March 22, 1991 (19910322)

ABSTRACT

PURPOSE: In a transistor wherein emitter and collector layers are constituted band gap materials wider than the base layer, to shorten the running time of a collector by providing a layer, which is of the same conductivity type as that of the base layer and is lower in impurity concentration than this, at a region where the collector contacts with the base layer.

CONSTITUTION: On a semiinsulating **InP** substrate 1 are stacked a collector layer 2, a base layer 3, and an emitter layer 4. The layer 2 consists of an N(sup +)- type **InP** third collector layer 2(sub 1), an N(sup -)-type **InP** second collector layer 2(sub 2), a P(sup -)-type **InP** first collector layer 2(sub 3), a P(sup -)-type InGaAsP layer 2(sub 4), and a P(sup -)-type **GaAs** layer 2(sub 5), and the layer

2(sub 4) changes the hand gap between the base layer 3 and the collector layer smoothly. Moreover, when the concentrations of the first - third collector layers are made N(sub 1)-N(sub 3), these relations are put ion N(sub 1)<N(sub 2)<N(sub 3). Moreover, for the layer 3, P(sup +)-type **InGaAs** is used, and the layer 4 consists of an N-type InGaAsP layer 4(sub 1), an N-type **InP** layer 4(sub 2), and an N(sup +)- type **InP** layer 4(sub 3), and the layer 4(sub 1) smoothes the gap between the base and the emitter.

32/3,AB/18 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

02299461
SEMICONDUCTOR DEVICE

PUB. NO.: 62-216361 [JP 62216361 A]
PUBLISHED: September 22, 1987 (19870922)
INVENTOR(s): FUJII TOSHIO
MUTO SHUNICHI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-058239 [JP 8658239]
FILED: March 18, 1986 (19860318)
JOURNAL: Section: E, Section No. 589, Vol. 12, No. 77, Pg. 57, March 10, 1988 (19880310)

ABSTRACT

PURPOSE: To increase a current gain by regulating the effective height of a barrier on which carrier moving in a **hetero junction** surface perpendicular direction overrides by selectively doping at barrier side.

CONSTITUTION: In an element using a **hetero junction** and utilizing a carrier circular transfer phenomenon perpendicular to the **hetero junction** surface, selective doping is performed at part of the junction at the side of a barrier layer to regulate the effective barrier on which the carrier overrides by generating the bent of a band. Since the selective doping is achieved at part of the hetero barrier layer and the height of the effective barrier on which the carrier tends to override is varied by utilizing the bent of the band generated from the result of the movements of electrons due to the difference of electron affinity, irregular lattice alignment is avoided, and lattice constant ratio .delta.A/A<=10(sup -3) can be, for example obtained. It can be applied to the **hetero junction** device of various compounds such as HET in which **InGaAs**, InAlAs are laminated on an **InP** substrate, or HET in which **GaAs**, InGaP are laminated on a **GaAs** substrate.

```
File    2:INSPEC  1969-2002/Mar W2
        (c) 2002 Institution of Electrical Engineers

Set     Items    Description
S1      37919    CI=(GA SS(S) AS SS)(S) NE=2
S2      18835    CI=(IN SS(S)GA SS(S)AS SS)(S)NE=3
S3        478    CI=(GA SS(S)AS SS(S)SB SS)(S)NE=3
S4        653    CI=(IN SS(S)GA SS(S)SB SS)(S)NE=3
S5       7441    CI=(IN SS(S)P SS)(S)NE=2
S6       2364    CI=(IN SS(S)AS SS(S)P SS)(S) NE=3
S7        478    CI=(GA SS(S)AS SS(S)SB SS)(S)NE=3
S8        147    CI=(IN SS(S)P SS(S)SB SS)(S)NE=3
S9      26169    HBT OR HBTS OR HETERO()JUNCTION? OR HETEROJUNCTION?
S10      1041    SCHOTTKY(2N)CONTACT
S11      9148    (TRENCH?? OR HOLE? ? OR GROOVE? OR CHANNEL OR EDGE? ? OR F-
              LUSH OR RIDGE?)(3N)(LAYER? OR FILM OR FILMS OR COAT????)
S12      8099    (BARRIER OR BLOCK? OR CONFIN?)(2N)(LAYER? OR FILM OR FILMS
              OR COAT????)
S13       158    (GRADED)(2N)( CHANNEL OR TRENCH?? OR HOLE? ? OR GROOVE? ? -
              OR CHANNEL OR EDGE? ? OR FLUSH OR RIDGE?)
S14     36300    BAND()GAP
S15     12223    S9 AND (S1 OR GAAS OR GA()AS)
S16      2288    S15 AND (S2 OR INGAAS OR (IN()GA(2W)AS))
S17        82    S16 AND S14
S18         6    S16 AND S10
S19        46    S16 AND S11
S20         7    S16 AND S13
S21        50    S16 AND S12
S22         1    S19 AND S14
S23         1    S21 AND S14
S24         0    S19 AND SOURCE()ELECTRODE
S25         0    S19 AND DRAIN()ELECTRODE
S26         0    S21 AND (DRAIN OR SOURCE)()ELECTRODE
S27         7    S20 NOT S18
S28        91    S19 OR S21
S29         2    S28 AND BAND()GAP
S30        60    S15 AND CONTACT()LAYER?
S31         2    S30 AND S14
S32         0    S30 AND S13
S33         3    S30 AND S12
S34         3    S30 AND S11
S35         8    (S31:S34) NOT (S18 OR S20 OR S22 OR S23 OR S27)
S36        29    S16 AND (S3 OR GAASSB OR (GA(2W)AS(2W)SB) OR S4 OR INGASB -
              OR (IN(2W)GA(2W)SB))
S37        29    S36 NOT (S18 OR S20 OR S22 OR S23 OR S27 OR S29 OR S35)
S38       282    S16 AND (S6 OR (IN(2W)AS(2W)P) OR S7 OR (GA(2W)AS(2W)SB) OR
                S8 OR (IN(2W)P(2W)SB))
S39         0    S38 AND S13
S40         9    S38 AND S12
S41         5    S38 AND S11
S42        14    S40 OR S41
S43        11    S42 NOT (S18 OR S20 OR S22 OR S23 OR S27 OR S29 OR S35 OR -
              S37)
S44       255    S16 AND (S6 OR (IN(2W)AS(2W)P))
S45        28    S16 AND (S7 OR (GA(2W)AS(2W)SB))
S46         6    S16 AND (S8 OR (IN(2W)P(2W)SB))
S47         1    S46 NOT (S18 OR S20 OR S22 OR S23 OR S27 OR S29 OR S35 OR -
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		S37)
S48	0	S45 NOT (S18 OR S20 OR S22 OR S23 OR S27 OR S29 OR S35 OR - S37 OR S46)
S49	0	S44 AND (DRAIN OR SOURCE)(2N)(ELECTRODE)
S50	0	S44 AND S13
S51	7	S44 AND S12
S52	4	S44 AND S11
S53	0	S44 AND S10
S54	15	S44 AND (BAND(2N)GAP)
S55	26	S51 OR S52 OR S54
S56	15	S55 NOT (S18 OR S20 OR S22 OR S23 OR S27 OR S29 OR S35 OR - S37 OR S43 OR S47)

? T S18/3,AB/1-4

18/3,AB/1
DIALOG(R)File 2:INSPEC

5800002 INSPEC Abstract Number: B9802-1350F-019
Title: Millimeter-wave power HEMTs
Author(s): Arai, S.; Tokuda, H.
Author Affiliation: Microwave Solid-State Dept., Toshiba Corp., Kawasaki, Japan
Journal: Solid-State Electronics Conference Title: Solid-State Electron. (UK) vol.41, no.10 p.1575-9
Publisher: Elsevier,
Publication Date: Oct. 1997 Country of Publication: UK
CODEN: SSELA5 ISSN: 0038-1101
SICI: 0038-1101(199710)41:10L.1575:MWPH;1-X
Material Identity Number: S068-97010
U.S. Copyright Clearance Center Code: 0038-1101/97/$17.00+0.00
Conference Title: Topical Workshop on Heterostructure Microelectronics
Conference Sponsor: Aerosp. Res. & Dev.; U.S. Air Force of Sci. Res
Conference Date: 18-21 Aug. 1996 Conference Location: Sapporo, Japan
Language: English
Abstract: There are two structures in millimeter-wave **heterojunction** FETs. One is a HEMT, mainly Pseudomorphic **InGaAs** HEMT (PE-HEMT) and the other is a **Heterojunction** FET (HFET), which uses n-AlGaAs and an n-**InGaAs** or **GaAs** layer as a **Schottky contact** and channel layer, respectively. Although a PM-HEMT is superior to HFET in terms of gain and higher operating frequency, it tends to have a lower breakdown voltage. Therefore, the two devices are used according to the required output power and operating frequencies. This article describes a comparison of the structures and their performances for both HFETs and PM-HEMTs. The power performance of the devices developed at Toshiba are demonstrated.
Subfile: B
Copyright 1998, IEE

18/3,AB/2
DIALOG(R)File 2:INSPEC

5650430 INSPEC Abstract Number: B9709-2550E-107
Title: Water-rinse as post-treatment for **GaAs**/AlGaAs selective dry etching
Author(s): Kohno, M.; Oikawa, H.; Asai, S.; Tsutsui, H.; Matsumura, T.; Nashimoto, Y.
Author Affiliation: ULSI Device Dev. Lab., NEC Corp., Shiga, Japan
Conference Title: Proceedings of the Symposium on High Speed III-V Electronics for Wireless Applications and the Twenty-Fifth State-of-the-Art Program on Compound Semiconductors (SOTAPOCS XXV) p.49-55
Editor(s): Ren, F.; Chu, S.N.G.; Wu, C.S.; Pearton, S.J.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1996 Country of Publication: USA x+345 pp.
Material Identity Number: XX96-02888
Conference Title: Proceedings of High Speed III-V Electronics for Wireless Applications/State of the Art Program on Compound Semiconductor (SOTAPOCS) XXV (ISBN 1 56677 165 X)

Conference Sponsor: Electrochem. Soc
Conference Date: 6-11 Oct. 1996 Conference Location: San Antonio, TX, USA
Language: English
Abstract: This paper describes water-rinse cleaning as post-dry-etching treatment for **GaAs**-based FETs. We investigated the removal of etching residue by the water rinse, by means of XPS, TOF-SIMS, TEM, and EDX measurements. Good Schottky contacts were fabricated upon water-rinsed Al/sub 0.2/Ga/sub 0.8/As using WSi gate electrodes. We applied the water-rinse treatment to fabricating Al/sub 0.2/Ga/sub 0.8/As/In/sub 0.15/Ga/sub 0.85/As pseudomorphic **heterojunction** FETs (HJFETs) with a recess gate structure, and obtained an excellent Vth uniformity (sigma Vth=35 mV) and a small Vth shift (200 mV) from the design value, over a 3-inch diameter wafer. Because of these features, together with its simplicity, the post-dry-etching water-rinse treatment provides high throughput and production yield for high-performance short-gate **GaAs** integrated circuits.
Subfile: B

18/3,AB/3
DIALOG(R)File 2:INSPEC

5274228 INSPEC Abstract Number: B9607-1350H-015
Title: Optically controlled coplanar transmission lines for adaptive microwave signal processing applications
Author(s): Kremer, R.; Jager, D.
Author Affiliation: Sonderforschungsbereich, Gerhard-Mercator-Univ. GH Duisburg Univ., Germany
Conference Title: 1995 International Semiconductor Conference. CAS`95 Proceedings (Cat. No.95TH8071) p.503-6
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA xviii+622 pp.
ISBN: 0 7803 2647 4 Material Identity Number: XX96-00281
U.S. Copyright Clearance Center Code: 0 7803 2647 4/95/$4.00
Conference Title: 1995 International Semiconductor Conference. CAS `95 Proceedings
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 11-14 Oct. 1995 Conference Location: Sinaia, Romania
Language: English
Abstract: Optically controlled wave propagation effects in coplanar transmission lines on semiconducting substrate are reviewed in this paper. In particular, distributed Schottky photodiodes are examined where a depletion layer is formed below the center conductor. Experimentally, phase shifts as high as 110 deg/mm at 9 GHz using an optical power of merely 50 mu W are obtained for an optimized InAlAs-**InGaAs**-InP heterostructure.
Subfile: B

18/3,AB/4
DIALOG(R)File 2:INSPEC

4863870 INSPEC Abstract Number: B9503-2560J-016
Title: Fully self-aligned InP/**InGaAs heterojunction** bipolar transistors grown by chemical beam epitaxy with a Schottky collector

Author(s): Pelouard, J.L.; Matine, N.; Pardo, F.; Sachelarie, D.; Benchimol, J.L.
Author Affiliation: L2M-CNRS, Bagneux, France
p.393-6
Publisher: IEEE, New York, NY, USA
Publication Date: May 1993 Country of Publication: USA xx+738 pp.
ISBN: 0 7803 0993 6
Conference Title: 1993 (5th) International Conference on Indium Phosphide and Related Materials
Conference Sponsor: IEEE; Societe des Electriciens et des Electroniciens
Conference Date: 19-22 April 1993 Conference Location: Paris, France
Language: English
Abstract: A new **HBT** design for reduction of parasitic effects has been developed to demonstrate the ability of ballistic and quasi-ballistic electron transport into the base to improve **HBT** dynamic behavior. To reduce both the transit time and the charging time of the base-collector junction electrons are collected by a **Schottky contact**. As a result the transistor must be collector-up. A fully self-aligned process has been developed for collector-up **HBTs**. This small cross-type **HBT** exhibits an attractive potential for fast dynamic behavior. Static behavior has been characterized on test structures grown by chemical beam epitaxy. It has been shown that current injected by the emitter-base junction flows mainly at junction perimeter. Also, it has been demonstrated that the extrinsic base must be over-doped by ion implantation to have small enough access resistance to the base for good dynamic behavior. Static current gains up to 50 have measured for the shortest junction perimeters.
Subfile: B

? T S18/3,AB/5-9

18/3,AB/5
DIALOG(R)File 2:INSPEC

4516536 INSPEC Abstract Number: B9312-2560S-026
Title: 12 GHz 0.68 dB **InGaAs**/AlGaAs pseudomorphic HEMT
Author(s): Chen Xiaojian; Liu Jun; Zheng Xuefan
Author Affiliation: Nanjing Electron. Devices Inst., China
Journal: Research & Progress of SSE vol.13, no.1 p.14-17
Publication Date: Feb. 1993 Country of Publication: China
CODEN: GDYJE2 ISSN: 1000-3819
Language: Chinese
Abstract: The authors report on the experimental results of the **InGaAs**/AlGaAs pseudomorphic HEMT. Its **heterojunction** structure was grown on the semi-insulating **GaAs** substrate by MBE. Using the processes with lowest damage, AuGeNi/Au/**GaAs** ohmic **contact**, Al/AlGaAs **Schottky** barrier, and polyimide protecting film, they have developed the **InGaAs**/AlGaAs PM-HEMT. Transconductance of the device is g/sub m/=280 mS/mm. The minimum noise figure and associated gain of the device are 0.68 dB and 7.0 dB at f=12 GHz, respectively.
Subfile: B

18/3,AB/6
DIALOG(R)File 2:INSPEC

4412251 INSPEC Abstract Number: B9307-2560S-008
Title: High power pseudomorphic double-**heterojunction** field effect transistors with 26 V gate-drain breakdown voltages
Author(s): Matsunaga, K.; Iwata, N.; Kuzuhara, M.
Author Affiliation: Kansai Electron. Res. Lab., NEC Corp., Shiga, Japan
Conference Title: Gallium Arsenide and Related Compounds 1992. Proceedings of the Nineteenth International Symposium p.749-54
Editor(s): Ikegami, T.; Hasegawa, F.; Takeda, Y.
Publisher: IOP, Bristol, UK
Publication Date: 1993 Country of Publication: UK xxv+963 pp.
ISBN: 0 7503 0250 X
U.S. Copyright Clearance Center Code: 0305-2346/93/$7.50+.00
Conference Date: 28 Sept.-2 Oct. 1992 Conference Location: Karuizawa, Japan
Language: English
Abstract: The authors report an n-AlGaAs/i-**InGaAs**/n-AlGaAs double-**heterojunction** field effect transistor (HJFET) with an undoped AlGaAs **Schottky contact** layer underneath double recessed n/sup +/-**GaAs**/n-**GaAs** dual cap layers. The fabricated 0.5 mu m gate length HJFET, having a 500 AA thick n-**GaAs** cap layer with a 2*10/sup 17/ cm/sup -3/ donor concentration, is found to have a gate-drain reverse breakdown voltage as high as 26 V and a 400 mA/mm maximum channel current. This FET has a relatively constant transconductance over a wide gate bias range with a maximum transconductance of 228 mS/mm. No drain current dispersion was observed. A maximum available gain of 4.5 dB at 20 GHz was attained under high drain-source voltage conditions. These results indicate that the developed FET has a great potential for high output power applications with high efficiencies.
Subfile: B

? T S27/3,AB/1-4

27/3,AB/1
DIALOG(R)File 2:INSPEC

6424641 INSPEC Abstract Number: A2000-02-7340L-003, B2000-01-0520F-077
Title: Improved double delta-doped **InGaAs/GaAs** heterostructures with symmetric **graded channel**
Author(s): Li, Y.J.; Shieh, H.M.; Su, J.S.; Kao, M.J.; Hsu, W.C.
Author Affiliation: Dept. of Electr. Eng., Nat. Cheng Kung Univ., Tainan, Taiwan
Journal: Materials Chemistry and Physics vol.61, no.3 p.266-9
Publisher: Elsevier,
Publication Date: 1 Nov. 1999 Country of Publication: Switzerland
CODEN: MCHPDR ISSN: 0254-0584
SICI: 0254-0584(19991101)61:3L.266:IDDD;1-O
Material Identity Number: D750-1999-013
U.S. Copyright Clearance Center Code: 0254-0584/99/$20.00
Language: English
Abstract: Improved delta-doped (delta -doped) **InGaAs/GaAs** field-effect transistors by grading both sides of the **InGaAs** channel are grown by metal-organic chemical vapor deposition. With the In composition linearly varied from x=0.18 at the **GaAs/InGaAs** heterointerface to x=0.25 at center of the **InGaAs** channel, significantly enhanced mobility due to reduced scattering is achieved when compared to that without graded heterostructure. A distinguishable two-dimensional electron gas from Shubnikov-de Hass (SdH) measurement is observed. Meanwhile, an improved extrinsic transconductance of 300 mS/mm with gate length of 1.2 mu m is obtained.
Subfile: A B
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27/3,AB/2
DIALOG(R)File 2:INSPEC

6053601 INSPEC Abstract Number: B9811-2560S-034
Title: Multiple pulse-doped channel AlGaAs/**InGaAs/GaAs** HFETs
Author(s): Lour, W.S.; Hung, L.T.; Chang, W.L.; Lia, C.Y.; Hsieh, J.L.
Author Affiliation: Dept. of Electr. Eng., Nat. Taiwan Ocean Univ., Keelung, Taiwan
Conference Title: Proceedings of the Twenty-Sixth State-of-the-Art Program on Compound Semiconductors (SOTAPOCS XXVI) p.195-201
Editor(s): Buckley, D.N.; Chu, S.N.G.; Hou, H.Q.; Sah, R.E.; Vilcot, J.P. ; Deen, M.J.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1997 Country of Publication: USA ix+322 pp.
ISBN: 1 56677 128 5 Material Identity Number: XX98-00791
Conference Title: Proceedings of the Twenty-Sixth State-of-the-Art Program on Compound Semiconductors (SOTAPOCS XXVI)
Conference Sponsor: Electrochem. Soc
Conference Date: 4-9 May 1997 Conference Location: Montreal, Que., Canada
Language: English
Abstract: This paper reports on the fabrication and characterization of multiple pulse-doped channel AlGaAs/**InGaAs/GaAs heterojuncti**

on field-effect transistors (HFET's). Multiple pulse-doped sheets, delta (n/sub 1/)=1.2*10/sup 12/ delta (n/sub 2/)=4*10/sup 11/, delta (n/sub 3/)=1*10/sup 11/ cm/sup -2/ from buffer to gate is used as an active channel. Typical drain-to-source and gate-to-drain breakdown voltages are larger than 25 V. The further enhancement in breakdown voltage is using the following methodology: 1) a strained AlGaAs insulator, 2) and **InGaAs** quantum-well like channel, and 3) less impurity scattering in the **graded** pulse-doped **channel**. The maximum transconductance is 160 mS/mm with an available current density of 250 mA/mm. Further increasing the delta (n/sub 1/) to 4*10/sup 12/ cm/sup -2/ the maximum transconductance is 165 mS/mm. The available current density is increased to 480 mA/mm. Moreover, their transconductance vs. gate voltage profiles display broad plateaus. The fabricated devices exhibit a small output conductance of 0.3 mS/mm. The evaluated open-drain voltage gain is as high as 500.

Subfile: B

27/3,AB/3

DIALOG(R)File 2:INSPEC

5905440 INSPEC Abstract Number: B9806-2560S-007

Title: Characteristics of doping- and composition-**graded** doped **channel** HFETs with AlGaAs gate insulator

Author(s): Hung, L.T.; Lour, W.S.

Author Affiliation: Dept. of Electr. Eng., Nat. Taiwan Ocean Univ., Keeling, Taiwan

Journal: Solid-State Electronics vol.42, no.3 p.363-8

Publisher: Elsevier,

Publication Date: March 1998 Country of Publication: UK

CODEN: SSELA5 ISSN: 0038-1101

SICI: 0038-1101(199803)42:3L.363:CDCG;1-4

Material Identity Number: S068-98003

U.S. Copyright Clearance Center Code: 0038-1101/98/$19.00+0.00

Language: English

Abstract: We review the recent investigation and comparison of **heterojunction** field-effect transistors (HFETs) with a variety of doped channels. The doped channels used in the studied HFETs include uniformly doped **GaAs**, **InGaAs**, composition-graded **InGaAs**/ **GaAs**, and doping-graded **InGaAs** channels. All of the devices have an undoped AlGaAs layer used as gate insulator. So, the parallel conduction and transconductance suppression could be avoided totally. In the case of uniformly doped-channel HFETs, an **InGaAs** channel exhibits better electron transport properties than a **GaAs** one, The corresponding extrinsic transconductance, breakdown voltage and output conductance are 130(152) mS mm/sup -1/, 17(15) V, and 2(0.3) mS mm/sup -1/ for a **GaAs** (an **InGaAs**) channel. Further improvement by using composition- or doping-**graded channel** , electron mobility, transconductance, and breakdown voltage are enhanced. We obtained a breakdown voltage larger than 25 V and a transconductance of 184 mS mm/sup -1/ with a large gate voltage swing of 3.0 V.

Subfile: B

27/3,AB/4

DIALOG(R)File 2:INSPEC

5568614 INSPEC Abstract Number: B9706-2560S-007
Title: Characterization of **graded** pulse-doped **channel** AlGaAs/ **InGaAs/GaAs heterojunction** field-effect transistors
Author(s): Lour, W.S.; Chen, H.R.; Hung, L.-T.
Author Affiliation: Dept. of Electr. Eng., Nat. Taiwan Ocean Univ., China
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) vol.36, no.3A p.975-9
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: March 1997 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(199703)36:3AL.975:CGPD;1-Z
Material Identity Number: F221-97006
Language: English
Abstract: This paper reports on the fabrication and characterization of **graded** pulse-doped **channel** AlGaAs/**InGaAs**/ **GaAs heterojunction** field-effect transistors (HFET's). Triple pulse-doped sheets, delta (n/sub 1/)=1.2*10/sup 12/, delta (n/sub 2/)=4*10/sup 11/, delta (n/sub 3/)=1*10/sup 11/ cm/sup -2/ from buffer to gate is used as an active channel. Typical drain-to-source and gate-to-drain breakdown voltages are larger than 25 V. The further enhancement; in breakdown voltage is using the following methodology: 1) a strained AlGaAs insulator: 2) an **InGaAs** quantum-well like channel, and 3) less impurity scattering in the **graded** pulse-doped **channel** . The maximum transconductance is 160 mS/mm with an available current density of 250 mA/mm. Further increasing the delta (n/sub 1/) to 4*10/sup 12/ cm/sup -2/; the maximum transconductance is 165 mS/mm. The available current density is increased to 480 mA/mm. Moreover, their transconductance vs. gate voltage profiles display broad plateaus. The fabricated devices exhibit a small output conductance of 0.3 mS/mm. The evaluated open-drain voltage gain is as high as 500. These results have better performances than those of i-AlGaAs/n/sup +/-**InGaAs** HFET's fabricated by our system.
Subfile: B

? T S27/3,AB/5-7

27/3,AB/5
DIALOG(R)File 2:INSPEC

5555415 INSPEC Abstract Number: B9705-2560R-106
Title: **InGaAs-GaAs** pseudomorphic heterostructure transistors prepared by MOVPE
Author(s): Liu Wenchau; Laih Lihwen; Tsai Junghui; Lin Kunwei; Cheng Chinchuan
Author Affiliation: Dept. of Electr. Eng., Nat. Cheng-Kung Univ., Tainan, Taiwan
Journal: Journal of Crystal Growth Conference Title: J. Cryst. Growth (Netherlands) vol.170, no.1-4 p.438-41
Publisher: Elsevier,
Publication Date: Jan. 1997 Country of Publication: Netherlands
CODEN: JCRGAE ISSN: 0022-0248
SICI: 0022-0248(199701)170:1/4L.438:IGPH;1-A
Material Identity Number: J037-97005
U.S. Copyright Clearance Center Code: 0022-0248/97/$17.00
Conference Title: 8th International Conference on Metalorganic Vapour Phase Epitaxy

Conference Date: 9-13 June 1996 Conference Location: Cardiff, UK
Language: English
Abstract: In this paper, we will demonstrate two new **InGaAs-GaAs** pseudomorphic heterostructure transistors prepared by MOVPE technology, i.e. **InGaAs-GaAs graded**-concentration doping-**channel** MIS-like field effect transistors (FET) and heterostructure-emitter and heterostructure-base (**InGaAs-GaAs**) transistors (HEHBT). For the doping-channel MIS-like FET, the graded In/sub 0.15/Ga/sub 0.85/As doping-channel structure is employed as the active channel. For a 0.8*100 mu m/sup 2/ gate device, a breakdown voltage of 15 V, a maximum transconductance of 200 mS/mm, and a maximum drain saturation current of 735 mA/mm are obtained. For the HEHBT, the confinement effect for holes is enhanced owing to the presence of **GaAs/InGaAs/GaAs** quantum wells. Thus, the emitter injection efficiency is increased and a high current gain can be obtained. Also, due to the lower surface recombination velocity of **InGaAs** base layers, the potential spike of the emitter-base (E-B) junction can be reduced significantly. This can provide a lower collector-emitter offset voltage. For an emitter area of 4.9*10/sup -5/ cm/sup 2/, the common emitter current gain of 120 and the collector-emitter offset voltage of 100 mV are obtained.
Subfile: B

27/3,AB/6
DIALOG(R)File 2:INSPEC

5527701 INSPEC Abstract Number: B9705-2530B-001
Title: Controllable drain cut-in voltage with strong negative differential resistance in **GaAs/InGaAs** real-space transfer heterostructure
Author(s): Jan-Shing Su; Wei-Chou Hsu; Yu-Shyan Lin; Wei Lin
Author Affiliation: Dept. of Electr. Eng., Nat. Cheng Kung Univ., Tainan, Taiwan
Journal: Applied Physics Letters vol.70, no.8 p.1002-4
Publisher: AIP,
Publication Date: 24 Feb. 1997 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(19970224)70:8L.1002:CDVW;1-F
Material Identity Number: A135-97010
U.S. Copyright Clearance Center Code: 0003-6951/97/70(8)/1002/3/$10.00
Language: English
Abstract: Three-terminal **GaAs/InGaAs/GaAs** pseudomorphic real-space transfer heterostructure employing **graded channel** as the emitter layer grown by low-pressure metal-organic chemical-vapor deposition has been fabricated. We observe controllable drain cut-in voltage characteristics with strong negative differential resistance. The largest peak-to-valley current ratio of the proposed device is about 33000 at room temperature. Moreover, we observe an energy exchange effect between electrons.
Subfile: B

27/3,AB/7
DIALOG(R)File 2:INSPEC

5446739 INSPEC Abstract Number: A9702-7340L-012, B9701-2560S-020

Title: Electron mobility characteristics of In/sub x/Ga/sub 1-x/As/InAlAs/InP high electron mobility transistor (HEMT) structures grown by molecular beam epitaxy

Author(s): Roh, D.-W.; Lee, H.-G.; Lee, J.-J.
Author Affiliation: Electron. & Telecommun. Res. Inst., Taejon, South Korea

Journal: Journal of Crystal Growth vol.167, no.3-4 p.468-72
Publisher: Elsevier,
Publication Date: Oct. 1996 Country of Publication: Netherlands
CODEN: JCRGAE ISSN: 0022-0248
SICI: 0022-0248(199610)167:3/4L.468:EMCI;1-7
Material Identity Number: J037-96021
U.S. Copyright Clearance Center Code: 0022-0248/96/$15.00
Language: English

Abstract: In/sub x/Ga/sub 1-x/As/In/sub 0.52/Al/sub 0.48/As/InP HEMT structures for low noise application were grown by MBE onto InP substrates. The purpose of this work is to enhance the electron mobility of **InGaAs** /InAlAs epilayers for InP-based HEMT devices by changing the epitaxial structure and growth process. The influence of the growth temperature profile, growth interruption, and structural parameters on the electrical characteristics have been systematically studied based on Hall measurements. The growth of the channel and spacer layer with interruption results in an increase of mobility due to an improvement of interface abruptness. To improve the mobility characteristics, graded and pseudomorphic In/sub x/Ga/sub 1-x/As were adopted as a channel layer. With the **graded** composition **channel** layer the mobilities of 11800 cm/sup 2//V.s (300 K) and 50900 cm/sup 2//V.s (77 K) were obtained near a spacer thickness of 30 AA and a sheet carrier density of 2.5.10/sup 12/ cm/sup -2/.

Subfile: A B

? T S29/3,AB/1-2

29/3,AB/1
DIALOG(R)File 2:INSPEC

6979840 INSPEC Abstract Number: A2001-16-0762-015, B2001-08-7230C-032
Title: Investigation of multi-color, broadband quantum well infrared photodetectors with digital graded superlattice barrier and linear-graded barrier for long wavelength infrared applications
Author(s): Lee, J.-H.; Li, S.S.; Tidrow, M.Z.; Liu, W.K.
Author Affiliation: Dept. of Electr. & Comput. Eng., Florida Univ., Gainesville, FL, USA
Journal: Infrared Physics & Technology Conference Title: Infrared Phys. Technol. (Netherlands) vol.42, no.3-5 p.123-34
Publisher: Elsevier,
Publication Date: June-Oct. 2001 Country of Publication: Netherlands
CODEN: IPTEEY ISSN: 1350-4495
SICI: 1350-4495(200106/10)42:3/5L.123:IMCB;1-K
Material Identity Number: F152-2001-003
U.S. Copyright Clearance Center Code: 1350-4495/2001/$20.00
Conference Title: QWIP 2000. Workshop on Quantum Well Infrared Photodetectors
Conference Date: 27-29 July 2000 Conference Location: Dana Point, CA, USA
Language: English
Abstract: We report four different **InGaAs** /AlGaAs multi-color, broadband (BB) quantum well infrared photodetectors (QWIPs) with digital graded superlattice barrier (DGSLB) and linear-graded barrier (LGB) for long wavelength infrared (LWIR) detection. The two DGSLB-QWIPs were grown using compositionally DGSLB structures with **GaAs**/Al/sub 0.15/Ga/sub 0.85/As material system to create a staircase-like **band gap** variation in the barrier region. A BB spectral response (7-16 mu m) was obtained under positive biases while a normal spectral response (lambda /sub p/=11 mu m) was obtained under negative biases in the BB-DGSLB-QWIP. A high sensitivity double barrier (DB)-DGSLB-QWIP with a thin undoped Al/sub 0.15/Ga/sub 0.85/As DB grown on both side of the quantum well has also been studied. A normal spectral response with peak wavelength at 12 mu m was obtained in this device under both positive and negative biases. In addition, two **InGaAs** /AlGaAs QWIPs using Al/sub x/Ga/sub 1-x/As LGB with and without AlGaAs DB layers have also been investigated. For the BB-LGB-QWIP, the BB spectral response was obtained under positive biases while the voltage-tunable multi-color detection with two peaks were obtained at negative biases. A very high responsivity was achieved in the DB-LGB-QWIP.
Subfile: A B

29/3,AB/2
DIALOG(R)File 2:INSPEC

03514568 INSPEC Abstract Number: A90008708
Title: Band-**edge** discontinuities of strained-**layer** In/sub x/Ga/sub 1-x/As/**GaAs heterojunctions** and quantum wells
Author(s): Niki, S.; Lin, C.L.; Chang, W.S.C.; Wieder, H.H.
Author Affiliation: Dept. of Electr. & Comput. Eng., California Univ.,

San Diego, La Jolla, CA, USA
Journal: Applied Physics Letters vol.55, no.13 p.1339-41
Publication Date: 25 Sept. 1989 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
Language: English
Abstract: The conduction-band discontinuity (Delta E/sub c/) and the **band-gap** offset (Delta E/sub gh/) of In/sub x/Ga/sub 1-x/As/ **GaAs** multiple quantum wells grown on **GaAs** substrates by molecular beam epitaxy are investigated for 0<x<0.3. The **band gap** of strained In/sub x/Ga/sub 1-x/As, determined from the excitonic transition of room-temperature transmission spectra, is found to be linearly dependent on x and is in good agreement with the calculated values. The **band-gap** offset is found to be Delta E/sub gh/=1.15x eV. The conduction-band offset, compiled from published data, is Delta E/sub c/=0.75x eV, and thus (Delta E/sub c// Delta E/sub gh/)=0.65 independent of x.
Subfile: A

T S35/3,AB/1-4

35/3,AB/1
DIALOG(R)File 2:INSPEC

7017137 INSPEC Abstract Number: A2001-19-4255P-016, B2001-10-4320J-016
Title: Room temperature operation of an electrically injected single-defect photonic bandgap microcavity surface emitting laser
Author(s): Sabarinathan, J.; Zhou, W.D.; Kochman, B.; Berg, E.; Qasaimeh, O.; Brock, T.; Pang, S.; Bhattacharya, P.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., Michigan Univ., Ann Arbor, MI, USA
Conference Title: LEOS 2000. 2000 IEEE Annual Meeting Conference Proceedings. 13th Annual Meeting. IEEE Lasers and Electro-Optics Society 2000 Annual Meeting (Cat. No.00CH37080) Part vol.1 p.370-1 vol.1
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA 2 vol. xxiii+898 pp.
ISBN: 0 7803 5947 X Material Identity Number: XX-2000-02816
U.S. Copyright Clearance Center Code: 0 7803 5947 X/2000/$10.00
Conference Title: LEOS 2000. 2000 IEEE Annual Meeting Conference Proceedings
Conference Date: 13-16 Nov. 2000 Conference Location: Rio Grande, Puerto Rico
Language: English
Abstract: We report here 0.9 mu m lasing in a p-n junction 2D photonic **band gap** (PBG) defect mode microcavity surface-emitting laser with electrical injection. The **GaAs** based device heterostructure is grown by metal-organic vapor phase epitaxy (MOVPE). It consists of an n+ **GaAs contact layer**, an n-type lower **GaAs**/Al/sub 0.8/Ga/sub 0.2/As distributed Bragg reflector (DBR) mirror, an undoped lambda cavity (lambda =0.94 mu m) region with two 70 AA pseudomorphic In/sub 0.15/Ga/sub 0.85/As wells in the middle and p-type AlGaAs and **contact layers** on the top. n- and p-type Al/sub 0.96/Ga/sub 0.04/As layers are also inserted on the respective sides of the cavity region for eventual lateral wet-oxidation during the processing of the device. The photoluminescence emission peak from the quantum wells is observed at 940 nm.
Subfile: A B

35/3,AB/2
DIALOG(R)File 2:INSPEC

6788954 INSPEC Abstract Number: B2001-01-4260-014
Title: Cylindrical microcavity light emitters realized with double-oxide-confinement or single-defect photonic bandgap crystals
Author(s): Zhou, W.D.; Sabarinathan, J.; Kochman, B.; Berg, E.; Qasaimeh, O.; Brock, T.; Pang, S.; Bhattacharya, P.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., Michigan Univ., Ann Arbor, MI, USA
Conference Title: 58th DRC. Device Research Conference. Conference Digest (Cat. No.00TH8526) p.115-16
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xii+176 pp.

ISBN: 0 7803 6472 4 Material Identity Number: XX-2000-02218
Conference Title: 58th DRC. Device Research Conference
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 19-21 June 2000 Conference Location: Denver, CO, USA
Language: English

Abstract: The confinement of light in one, two, and three dimensions on a wavelength-scale can lead to light emitting devices with enhanced efficiency, narrow spectral linewidth, improved directionality, and even enhanced spontaneous recombination rate (Yokoyama, 1992). In this paper, we describe the design, fabrication and characteristics of electroluminescent cylindrical microcavity surface emitters realized either by double oxide confinement or as a photonic bandgap (PBG) microcavity. In the latter, a single "point defect" in a 2D photonic crystal traps light and serves as a true microcavity. Comparison of different lateral confinement structures is made. Double oxide-confined devices are made with InP-based heterostructures (lambda =1.55 mu m) and consist of either InGaAs (bulk) or InGaAsP-InP pseudomorphic MQW recombination regions buried in InGaAsP or InP spacers of thickness lambda /n. 120 nm thick In/sub 0.52/Al/sub 0.48/As layers are incorporated on both top and bottom of the cavity and appropriate p-type (top) and n-type (bottom) **contact layers** are included on both sides. The lateral microcavity size, defined by oxide confinement, ranges from 1 mu m to 30 mu m. PBG-based devices are made with **GaAs** -based heterostructures, which consist of an InGaAs MQW lambda -cavity (lambda =0.94 mu m). The 2D PBG formation is achieved by e-beam lithography and deep dry etching techniques. Single or multiple defects in the center define the lambda -sized microcavity. The PBG was designed to be centered around the cavity peak emission wavelength at 0.94 mu m.
Subfile: B

35/3,AB/3
DIALOG(R)File 2:INSPEC

6039749 INSPEC Abstract Number: B9811-2560J-025
Title: Effect of base metal contacts on the performance of InGaP/ **GaAs HBTs** under temperature and bias stress
Author(s): Bashar, S.A.; Sheng, H.; Amin, F.A.; Rezazadeh, A.A.; Crouchl, M.A.; Adami, F.; Cattani, L.
Author Affiliation: Dept. of Electron. Eng., King's Coll., London, UK
Conference Title: IEEE MTT/ED/AP/LEO Societies Joint Chapter United Kingdom and Republic of Ireland Section. 1997 Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications. EDMO (Cat. No.97TH8305) p.285-90
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA x+357 pp.
ISBN: 0 7803 4135 X Material Identity Number: XX98-00908
U.S. Copyright Clearance Center Code: 0 7803 4135 X/97/$5.00
Conference Title: IEEE MTT/ED/AP/LEO Societies Joint Chapter United Kingdom and Republic of Ireland Section. 1997 Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications EDMO
Conference Sponsor: IEEE Electron Devices Soc.; IEEE Microwave Theory & Tech. Soc.; IEEE Lasers & Electro-Opt. Soc.; IEE; IOP
Conference Date: 24-25 Nov. 1997 Conference Location: London, UK
Language: English
Abstract: A wide range of base ohmic contacts have been studied to determine each of their suitability for usage in InGaP/**GaAs HBTs** for operation at high temperature. A novel base ohmic contact

using Ti/ZrB/sub 2//Au has been developed with ZrB/sub 2/ as a **barrier layer** to prevent Au indiffusion from the **contact layer** to the base region. Current stress at high temperature on these **HBTs** show that the devices with this novel contact remain unchanged beyond 20 hours whereas devices with conventional contacts show clear signs of degradation after only a few hours of stress.
Subfile: B

35/3,AB/4
DIALOG(R)File 2:INSPEC

5978020 INSPEC Abstract Number: B9809-2560R-009
Title: Performance of a p-channel **heterojunction** FET with P/sup +/- **GaAs** selectively grown **contact layers** for **GaAs** complementary ICs
Author(s): Furuhata, N.; Fujit, M.; Asai, S.; Maeda, T.; Ohno, Y.
Author Affiliation: Optoelectron. & High Frequency Device Res. Lab., Ibaraki, Japan
Journal: Solid-State Electronics vol.42, no.6 p.1049-55
Publisher: Elsevier,
Publication Date: June 1998 Country of Publication: UK
CODEN: SSELA5 ISSN: 0038-1101
SICI: 0038-1101(199806)42:6L.1049:PCHW;1-M
Material Identity Number: S068-98006
U.S. Copyright Clearance Center Code: 0038-1101/98/$19.00+0.00
Language: English
Abstract: A new p-channel **heterojunction** field-effect transistor (HJFET) for **GaAs** complementary ICs is proposed. The device is a doped-channel metal-insulator-semiconductor (MIS) structure with an i-AlGaAs **barrier layer** of high Al mole fraction to suppress gate forward leakage. Its source-drain regions are formed by p/sup +/- **GaAs**, layers selectively grown by metalorganic molecular beam epitaxy (MOMBE) to reduce parasitic resistance. The 0.5 mu m HJFET exhibits a maximum transconductance of 40 mS mm/sup -1/, a gate leakage turn-on voltage of -1.2 V, a cut-off frequency of 6.8 GHz, and a maximum frequency of oscillation of 8.0 GHz. Its source resistance of 10 n mm is half of that for a device structure without selectively grown **contact layers** . Moreover, performances of **GaAs** complementary ICs, using this p-channel HJFET and a previously reported 0.5 mu m n-channel HJFET, are estimated by SPICE. As a result, a propagation delay of 120 ps and a power dissipation of 0.08 mu W MHz/sup -1/ gate/sup -1/ at a 1.0 V supply voltage are predicted.
Subfile: B

? T S35/3,AB/5-8

35/3,AB/5
DIALOG(R)File 2:INSPEC

5419353 INSPEC Abstract Number: B9612-2560J-014
Title: Evaluation of molecular beam epitaxially grown AlGaAs/**GaAs** **heterojunctions** for bipolar transistor with InGaAs emitter **contact layer**
Author(s): Izumi, S.; Sakai, M.; Shimura, T.; Hayafuji, N.; Sato, K.;

Otsubo, M.
Author Affiliation: Optoelectron. & Microwave Devices R&D Lab., Mitsubishi Electr. Corp., Hyogo, Japan
Journal: Applied Physics Letters vol.69, no.17 p.2516-18
Publisher: AIP,
Publication Date: 21 Oct. 1996 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(19961021)69:17L.2516:EMBE;1-K
Material Identity Number: A135-96044
U.S. Copyright Clearance Center Code: 0003-6951/96/69(17)/2516/3/$10.00
Language: English
Abstract: Molecular beam epitaxially grown AlGaAs/**GaAs heterojunctions** were characterized by isothermal capacitance transient spectroscopy to study the performance of bipolar transistors with lattice-mismatched InGaAs emitter **contact layer**. A deep level around 0.48 eV is found to be a recombination center in the N-AlGaAs/p/sup +/-**GaAs** junction which might be induced by oxygen. Anomalous signals are also observed under an isothermal condition where the **edge** of the depletion **layer** reaches the graded InGaAs/AlGaAs heterointerface. Two electron traps with activation energies of 0.26 and 0.62 eV are identified as dominant factors.
Subfile: B

35/3,AB/6
DIALOG(R)File 2:INSPEC

5231790 INSPEC Abstract Number: B9605-1350F-043
Title: A Q-band 1 watt 30% power-added-efficiency **hetero-junction** FET
Author(s): Arai, S.; Mizuno, H.; Tanaka, H.; Yoshinaga, H.; Masuda, K.; Abe, B.; Kawano, M.; Tokuda, H.; Shibata, K.
Author Affiliation: Komukai Works, Toshiba Corp., Kawasaki, Japan
Conference Title: GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. 17th Annual Technical Digest 1995 (Cat. No.95CH35851) p.296-9
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA xix+330 pp.
ISBN: 0 7803 2966 X Material Identity Number: XX95-02876
U.S. Copyright Clearance Center Code: 0 7803 2966 X/95/$4.00
Conference Title: GaAs IC Symposium IEEE Gallium Arsenide Integrated Circuit Symposium 17th Annual Technical Digest 1995
Conference Sponsor: IEEE Electron Devices Soc.; IEEE Microwave Theory & Tech. Soc
Conference Date: 29 Oct.-1 Nov. 1995 Conference Location: San Diego, CA, USA
Language: English
Abstract: A series of Q-band **hetero-junction** power FETs with gate widths of 400, 800, 1600 and 2400 mu m has been developed. The FETs use an n-type **GaAs layer** as a **channel** with an AlGaAs **layer** as a Schottky **contact layer**. Each FET has two cell configuration with monolithically integrated 1/4 wavelength impedance transformer for the input and output matching networks. The 2400 mu m-gate-width device delivered an output power of 30 dBm with 4.4 dB gain and 30.1% power-added-efficiency.
Subfile: B

35/3,AB/7
DIALOG(R)File 2:INSPEC

04196438 INSPEC Abstract Number: B9209-2560J-009
Title: Growth of **GaAs**/AlGaAs **HBTs** by MOMBE (CBE)
Author(s): Abernathy, C.R.; Ren, F.; Pearton, S.J.; Fullowan, T.R.; Montgomery, R.K.; Wisk, P.W.; Lothian, J.R.; Smith, P.R.; Nottenburg, R.N.
Author Affiliation: AT&T Bell Labs., Murray Hill, NJ, USA
Journal: Journal of Crystal Growth vol.120, no.1-4 p.234-9
Publication Date: May 1992 Country of Publication: Netherlands
CODEN: JCRGAE ISSN: 0022-0248
U.S. Copyright Clearance Center Code: 0022-0248/92/$05.00
Conference Title: 3rd International Conference on Chemical Beam Epitaxy and Related Growth Techniques (ICCBE-3)
Conference Sponsor: British Assoc. Crystal Growth; IOP; Eur. Office US Army; Eur. Office US Air Force
Conference Date: 1-5 Sept. 1991 Conference Location: Oxford, UK
Language: English
Abstract: The authors discuss how the unique growth chemistry of MOMBE can be used to produce high speed **GaAs**/AlGaAs **heterojunction** bipolar transistors (**HBTs**). The ability to grow heavily doped, well-**confined layers** with carbon doping from trimethylgallium (TMG) is a significant advantage for this device. However, in addition to high p-type doping, high n-type doping is also required. While elemental Sn can be used to achieve doping levels up to 1.5*10/sup 19/ cm/sup -3/, severe segregation limits its use to surface **contact layers**. With tetraethyltin (TESn), however, segregation does not occur and Sn doping can be used throughout the device. Using these sources along with triethylgallium (TEG), trimethylamine alane (TMAA), and AsH/sub 3/, the authors have fabricated Npn devices with 2 mu m*10 mu m emitter stripes which show gains of >or=20 with either f/sub t/=55 GHz and f/sub max/=70 GHz or f/sub t/=70 GHz and f/sub max/=50 GHz, depending upon the structure.
Subfile: B

35/3,AB/8
DIALOG(R)File 2:INSPEC

01155665 INSPEC Abstract Number: B78010344
Title: Normally-off Al/sub 0.5/Ga/sub 0.5/As **heterojunction**-gate **GaAs** f.e.t
Author(s): Morkoc, H.; Bandy, S.G.; Antypas, G.A.; Sankaran, R.
Author Affiliation: Corporate Solid State Lab., Varian Associates Inc., Palo Alto, CA, USA
Journal: Electronics Letters vol.13, no.24 p.747-8
Publication Date: 24 Nov. 1977 Country of Publication: UK
CODEN: ELLEAK ISSN: 0013-5194
Language: English
Abstract: DC microwave and large-signal switching properties of a normally-off **heterojunction**-gate **GaAs** f.e.t. are reported. The device structure comprises an n-type active **channel layer**, a p-type, Al/sub 0.5/Ga/sub 0.5/As gate layer and a p/sup +/-layer **GaAs** **contact layer** . The gate structure is obtained by selectively etching the p-type **GaAs** and Al/sub 0.5/Ga/sub 0.5/As. Undercutting of the Al/sub 0.5/Ga/sub 0.5/As layer results in a submicrometre gate length,

and the resulting p/sup +/-**GaAs** overhand is used to self align the source and the drain with respect to the gate. **GaAs** f.e.t.s with 0.5 to 0.7 mu m-long **heterojunction** gates have exhibited maximum available power gains of about 9 dB at 2 GHz. Large-signal pulse measurements indicate an intrinsic propagation delay of 40 ps with an arbitrarily chosen 100 Omega drain load resistance in a 50 Omega microstrip circuit.

Subfile: B

37/3,AB/2
DIALOG(R)File 2:INSPEC

6850971 INSPEC Abstract Number: A2001-07-7340L-002
Title: Mesoscopic conductance oscillations associated with dislocations in semiconductors
Author(s): Figielski, T.; Wosinski, T.; Makosa, A.
Author Affiliation: Inst. of Phys., Polish Acad. of Sci., Warsaw, Poland
Journal: Physica Status Solidi B vol.222, no.1 p.151-8
Publisher: Wiley-VCH,
Publication Date: 1 Nov. 2000 Country of Publication: Germany
CODEN: PSSBBD ISSN: 0370-1972
SICI: 0370-1972(20001101)222:1L.151:MCOA;1-T
Material Identity Number: P107-2000-012
U.S. Copyright Clearance Center Code: 0370-1972/2000/$17.50+0.50
Language: English
Abstract: In this paper, we demonstrate that dislocations in a macroscopic semiconductor specimen can give rise to specific mesoscopic effects. In the first place, we compare with each other two kinds of closed electron orbits that can appear in small specimens of metals and semiconductors in a magnetic field: the cyclotron orbits and the Aharonov-Bohm orbits. Next, we consider possible Aharonov-Bohm orbits encircling a dislocation in a semiconductor under a strong magnetic field whose direction is aligned with the dislocation axis. Finally, we demonstrate experiments confirming the formation of such orbits around misfit dislocations in semiconductor heterostructures with a small lattice mismatch. They manifest themselves at low temperatures as regular fluctuations of conductance through a heterostructure, appearing as a function of applied voltage and magnetic field.
Subfile: A

37/3,AB/3
DIALOG(R)File 2:INSPEC

6801767 INSPEC Abstract Number: A2001-03-7340L-007
Title: Deep-level defects at lattice-mismatched interfaces in **GaAs** -based **heterojunctions**
Author(s): Wosinski, T.; Yastrubchak, O.; Makosa, A.; Figielski, T.
Author Affiliation: Inst. of Phys., Polish Acad. of Sci., Warsaw, Poland
Journal: Journal of Physics: Condensed Matter Conference Title: J. Phys., Condens. Matter. (UK) vol.12, no.49 p.10153-60
Publisher: IOP Publishing,
Publication Date: 11 Dec. 2000 Country of Publication: UK
CODEN: JCOMEL ISSN: 0953-8984
SICI: 0953-8984(20001211)12:49L.10153:DLDL;1-K
Material Identity Number: M789-2000-050
U.S. Copyright Clearance Center Code: 0953-8984/2000/4910153+08$30.00
Conference Title: Extended Defects in Semiconductors 2000
Conference Date: 18-22 July 2000 Conference Location: Brighton, UK
Language: English
Abstract: Electrical properties of lattice-mismatch-induced defects in **GaAs/GaAsSb** and **GaAs/InGaAs heterojunctions** have been studied by means of an electron-beam-induced current (EBIC) in a scanning electron microscope and deep-level transient spectroscopy (DLTS).

DLTS measurements, carried out with p-n junctions formed at the interfaces, revealed one electron trap and two hole traps induced by the lattice mismatch. The electron trap, at about E/sub c/-0.68 eV, has been attributed to electron states associated with threading dislocations in the ternary compound. By comparing the concentration of this trap, revealed by DLTS, with EBIC results on the diffusion length, obtained for **heterojunctions** with different lattice mismatches, it is inferred that the minority-carrier lifetime is controlled by dislocations in the epilayer region close to the interface. Two new hole traps have been ascribed to defects associated with the lattice-mismatched interface of the heterostructures.

Subfile: A

? T S37/3,AB/4-9

37/3,AB/4

DIALOG(R)File 2:INSPEC

6697048 INSPEC Abstract Number: B2000-10-0520D-082

Title: Integrated multiple sensor controlled molecular beam epitaxy for high performance electronic devices

Author(s): Chow, D.H.; Roth, J.A.; Thomas, S., III; Kiziloglu, K.; Fields, C.H.; Arthur, A.; Enquist, P.M.; Fountain, G.; Reed, F.; Johs, B.; Olson, G.L.; Williamson, W.S.

Author Affiliation: HRL Labs., Malibu, CA, USA

Conference Title: Conference Proceedings. 2000 International Conference on Indium Phosphide and Related Materials (Cat. No.00CH37107) p.33-6

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2000 Country of Publication: USA x+582 pp.

ISBN: 0 7803 6320 5 Material Identity Number: XX-2000-01356

U.S. Copyright Clearance Center Code: 0 7803 6320 5/2000/$10.00

Conference Title: Conference Proceedings. 2000 International Conference on Indium Phosphide and Related Materials

Conference Sponsor: IEEE Electron Devices Soc.; IEEE Lasers & Electro-Opt. Soc

Conference Date: 14-18 May 2000 Conference Location: Williamsburg, VA, USA

Language: English

Abstract: We report the application of sensor-controlled molecular beam epitaxy (MBE) to the development of integrated electronic devices, specifically **heterojunction** bipolar transistors (**HBTs**) and resonant tunneling diodes (RTDs), for high performance circuits on InP substrates. Of particular importance for the integration of RTDs into a high performance circuit architecture is control of peak current density, J/sub p/, which depends exponentially on quantum barrier layer thickness (roughly a factor of 2 change in peak current density per monolayer). Using a combination of spectroscopic ellipsometry and photoemission oscillation sensors, we have developed a real-time control process for AlAs barriers in In/sub 0.53/Ga/sub 0.47/As/AlAs/InAs RTDs with +or-0.1 monolayer precision (+or-7% in J/sub p/). Key process control capabilities for reproducible deposition of **HBT** device structures are substrate temperature control (based on absorption edge spectroscopy), and ternary alloy composition control (based on spectroscopic ellipsometry). We report here the successful integration of two distinct **HBT** structures with RTDs on InP. In the first case, we have demonstrated good yield and RF performance (f/sub t/>75 GHz, f/sub max/>150 GHz) from HRL's baseline Ga/sub 0.47/In/sub 0.53/As/Al/sub 0.48/In/sub 0.52/As **HBTs** integrated with

RTDs in a stacked geometry. In the second case, we have demonstrated high DC gain (40-50), high breakdown voltages (>4 V), and good RF performance (f/sub t/>100 GHz) from Al/sub 0.48/In/sub 0.52/As/**GaAs** /sub 0.5/Sb/sub 0.5/ **HBTs** integrated with RTDs using Research Triangle Institute's Symmetric Intrinsic Process.

Subfile: B

37/3,AB/5

DIALOG(R)File 2:INSPEC

6481573 INSPEC Abstract Number: A2000-05-7335C-003, B2000-03-2530B-009

Title: Spin-dependent resonant tunneling in semiconductor nanostructures

Author(s): Andrada e Silva, E.A.; La Rocca, G.C.

Author Affiliation: Inst. Nacional de Pesquisas Espaciais, Sao Paulo, Brazil

Journal: Brazilian Journal of Physics Conference Title: Braz. J. Phys. (Brazil) vol.29, no.4 p.719-22

Publisher: Soc. Brasileira de Fis,

Publication Date: Dec. 1999 Country of Publication: Brazil

CODEN: BJPHE6 ISSN: 0103-9733

SICI: 0103-9733(199912)29:4L.719:SDRT;1-T

Material Identity Number: P825-2000-001

Conference Title: 9th Brazilian Workshop on Semiconductor Physics

Conference Sponsor: Fundacaoo de Amparo a Pesquisa do Estado de Minas Gerais; Conselho Nacional de Desenvolvimento Cientifico e Technol.; et al

Conference Date: 7-12 Feb. 1999 Conference Location: Belo Horizonte, Brazil

Language: English

Abstract: The spin-dependent quantum transport of electrons in nonmagnetic III-V semiconductor nanostructures is studied theoretically within the envelope function approximation and the Kane model for the bulk. It is shown that an unpolarized beam of conducting electrons can be strongly polarized in zero magnetic field by resonant tunneling across asymmetric double-barrier structures, as an effect of the spin-orbit interaction. The electron transmission probability is calculated as a function of energy and angle of incidence. Specific results for tunneling across lattice matched politype Ga/sub 0.47/In/sub 0.53/As/InP/Ga/sub 0.47/In/sub 0.53/As/**GaAs** /sub 0.5/Sb/sub 0.5//Ga/sub 0.47/In/sub 0.53/As double barrier heterostructures show sharp spin split resonances, corresponding to resonant tunneling through spin-orbit split quasi-bound electron states. The polarization of the transmitted beam is also calculated and is shown to be over 50%.

Subfile: A B

37/3,AB/6

DIALOG(R)File 2:INSPEC

6467337 INSPEC Abstract Number: B2000-02-2560J-028

Title: InP/**GaAsSb**/InP double **heterojunction** bipolar transistors with high cut-off frequencies and breakdown voltages

Author(s): Matine, N.; Dvorak, M.W.; Xu, X.G.; Watkins, S.P.; Bolognesi, C.R.

Author Affiliation: Dept. of Phys., Simon Fraser Univ., Burnaby, BC,

Canada
Conference Title: Conference Proceedings. Eleventh International Conference on Indium Phosphide and Related Materials (IPRM'99) (Cat. No.99CH36362) p.179-82
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA (ix+588+31 suppl.) pp.
ISBN: 0 7803 5562 8 Material Identity Number: XX-1999-01493
U.S. Copyright Clearance Center Code: 0 7803 5562 8/99/$10.00
Conference Title: Conference Proceedings. Eleventh International Conference on Indium Phosphide and Related Materials (IPRM'99)
Conference Sponsor: Swiss Sect. IEEE; IEEE Laser & Electro-Opt. Soc.; IEEE Electron Devices Soc
Conference Date: 16-20 May 1999 Conference Location: Davos, Switzerland
Language: English
Abstract: In this work, we report on the DC and microwave performance of MOCVD-grown carbon-doped InP/**GaAsSb**/InP double **heterojunction** transistors (DHBTs) with various collector thicknesses. The cut-off frequencies (and breakdown voltages) are 106 GHz (8 V), 82 GHz (10 V) and 40 GHz (15 V) for the 2000 AA, 3000 AA and 5000 AA, lightly doped collectors. The 106 GHz, which is the best f/sub T/ ever reported in this material system, is obtained while maintaining a relatively high breakdown voltage (BV/sub CEO/=8 V). The lower cut-off frequencies obtained for the 3000 AA and 5000 AA, collectors are attributed to the longer transit time in the collector and also to the Kirk like limitation brought about by high current densities in the thicker collectors.
Subfile: B

37/3,AB/7
DIALOG(R)File 2:INSPEC

6426200 INSPEC Abstract Number: A2000-02-7865K-013, B2000-01-2530B-020
Title: Electroluminescence and photoelectric properties of type II broken-gap n-**In**(**Ga**)**As**(**Sb**)/N-GaSb heterostructures
Author(s): Moiseev, K.D.; Mikhailova, M.P.; Stoyanov, N.D.; Yakovlev, Yu.P.; Hulicius, E.; Simecek, T.; Oswald, J.; Pangrac, J.
Author Affiliation: A.F. Ioffe Physicotech. Inst., Acad. of Sci., St. Petersburg, Russia
Journal: Journal of Applied Physics vol.86, no.11 p.6264-8
Publisher: AIP,
Publication Date: 1 Dec. 1999 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
SICI: 0021-8979(19991201)86:11L.6264:EPPT;1-Q
Material Identity Number: J004-1999-022
U.S. Copyright Clearance Center Code: 0021-8979/99/86(11)/6264(5)/$15.00
Language: English
Abstract: Layers of n-InAs and n-InGaAsSb were grown by metalorganic vapor phase epitaxy and liquid phase epitaxy on N-GaSb substrates. The electroluminescence, current-voltage characteristics and photocurrent spectra of these heterostructures were studied at low temperatures. It was shown that GaSb/**In**(**Ga**)**As**(**Sb**) with InAs-rich narrow-gap solid solutions are broken-gap **heterojunctions** of type II at 77 and 300 K. Intense electroluminescence of the N-GaSb/n-**In**(**Ga**)**As**(**Sb**) heterostructures was found in the spectral range of 3-4 mu m at 77 K. The origin of radiative recombination at the N-n

type II broken-gap heterointerface is proposed and is in agreement with the experimental results for both systems.
Subfile: A B

37/3,AB/8
DIALOG(R)File 2:INSPEC

6334391 INSPEC Abstract Number: A1999-19-7865K-034, B1999-10-0520D-140
Title: Optical properties of **GaAs**/sub 0.5/Sb/sub 0.5/ and In/sub 0.53/Ga/sub 0.47/As/**GaAs** /sub 0.5/Sb/sub 0.5/ type II single hetero-structures lattice-matched to InP substrates grown by molecular beam epitaxy
Author(s): Yamamoto, A.; Kawamura, Y.; Naito, H.; Inoue, N.
Author Affiliation: Res. Inst. for Adv. Sci. & Technol., Osaka Prefecture Univ., Japan
Journal: Journal of Crystal Growth Conference Title: J. Cryst. Growth (Netherlands) vol.201-202 p.872-6
Publisher: Elsevier,
Publication Date: May 1999 Country of Publication: Netherlands
CODEN: JCRGAE ISSN: 0022-0248
SICI: 0022-0248(199905)201/202L.872:OPG5;1-Z
Material Identity Number: J037-1999-011
U.S. Copyright Clearance Center Code: 0022-0248/99/$20.00
Conference Title: Molecular Beam Epitaxy 1998. Tenth International Conference
Conference Date: 31 Aug.-4 Sept. 1998 Conference Location: Cannes, France
Language: English
Abstract: **GaAs**/sub 0.5/Sb/sub 0.5/ and In/sub 0.53/Ga/sub 0.47/As/ **GaAs** /sub 0.5/Sb/sub 0.5/ single hetero (SH) structures were grown by molecular beam epitaxy. It was found that the PL spectrum of the **GaAsSb** layers shows a remarkable dependence on the growth temperature and the V/III ratio. A sharp single-peak PL spectrum was obtained for the **GaAsSb** when the V/III ratio was 12.0 and the growth temperature was 505 degrees C. In addition, a below gap type II emission at 2.4-2.5 mu m was observed at 77 K for the **InGaAs/GaAsSb** SH structure for the first time.
Subfile: A B

37/3,AB/9
DIALOG(R)File 2:INSPEC

6293294 INSPEC Abstract Number: A1999-16-7335C-004
Title: Electron-spin polarization by resonant tunneling
Author(s): de Andrada e Silva, E.A.; La Rocca, G.C.
Author Affiliation: Inst. Nacional de Pesquisas Espaciais, Sao Paulo, Brazil
Journal: Physical Review B (Condensed Matter) vol.59, no.24 p. R15583-5
Publisher: APS through AIP,
Publication Date: 15 June 1999 Country of Publication: USA
CODEN: PRBMDO ISSN: 0163-1829
SICI: 0163-1829(19990615)59:24L.r15583:ESPR;1-L

Material Identity Number: P279-1999-024
U.S. Copyright Clearance Center Code: 0163-1829/99/59(24)/15583(3)/$15.00
Language: English

Abstract: The spin-dependent electron resonant tunneling through nonmagnetic III-V semiconductor asymmetric double barriers is studied theoretically within the envelope function approximation and the Kane model for the bulk. It is shown, in particular, that an unpolarized beam of conducting electrons can be strongly polarized, at zero magnetic field, by a spin-dependent resonant tunneling, due to the Rashba mesoscopic spin-orbit interaction. The electron transmission probability is calculated as a function of the electron's energy and angle of incidence. Specific results for tunneling across lattice matched politype Ga/sub 0.47/In/sub 0.53/As/InP/Ga/sub 0.47/In/sub 0.53/As/**GaAs** /sub 0.5/ Sb/sub 0.5//Ga/sub 0.47/In/sub 0.53/As double barrier nanostructures show, for instance, sharp spin-split resonances, corresponding to resonant tunneling through spin-orbit split quasibound ground and excited electron states (quasisubbands). The calculated polarization of the transmitted beam in resonance with the second quasisubband shows that polarization bigger than 50% can be achieved with this effect.

Subfile: A

37/3,AB/10
DIALOG(R)File 2:INSPEC

6102199 INSPEC Abstract Number: A9902-7125T-006
Title: Energy bandgap of Al/sub x/Ga/sub 1-x/As/sub 1-y/Sb/sub y/ and conduction band discontinuity of Al/sub x/Ga/sub 1-x/As/sub 1-y/Sb/sub y//InAs and Al/sub x/Ga/sub 1-x/As/sub 1-y/Sb/sub y//**InGaAs** heterostructures
Journal: Solid-State Electronics vol.42, no.11 p.2101-4
Publisher: Elsevier,
Publication Date: Nov. 1998 Country of Publication: UK
CODEN: SSELA5 ISSN: 0038-1101
SICI: 0038-1101(199811)42:11L.2101:EBAX;1-G
Material Identity Number: S068-98010
U.S. Copyright Clearance Center Code: 0038-1101/98/$19.00+0.00
Language: English
Abstract: A technique to determine the conduction band discontinuity in any heterostructure and the resulting band alignment is presented. Energy bandgaps of the quaternary AlGaAsSb and conduction band discontinuity for lattice matched Al/sub x/Ga/sub 1-x/As/sub 1-y/Sb/sub y//InAs, Al/sub x/Ga/sub 1-x/As/sub 1-y/Sb/sub y//In/sub 0.8/Ga/sub 0.2/As and Al/sub x/Ga/sub 1-x/As/sub 1-y/Sb/sub y//In/sub 0.52/Ga/sub 0.48/As heterostructures are reported for varying Al and Sb mole fractions to demonstrate the method. Al/sub x/Ga/sub 1-x/As/sub 1-y/Sb/sub y//InAs changes from a type-II broken-gap alignment to type-II staggered alignment near an Al mole fraction of 0.15 followed by a change from type-II to type-I near an Al mole fraction of 0.9. No type-II broken-band alignments are observed in the other two lattice matched systems. The minimum Al mole fraction required for type-I band alignment increases with increasing In mole fraction. It is shown that the quaternary bandgap becomes indirect for Al mole fractions greater than approximately 0.4 and the conduction band discontinuity is a linear function of the Al mole fraction for the lattice-matched systems.
Subfile: A

37/3,AB/11
DIALOG(R)File 2:INSPEC

6090855 INSPEC Abstract Number: A9901-6855-113, B9901-0520J-003
Title: Multicomponent Sb-based solid solutions grown from Sb-rich liquid phases
Author(s): Mishurnyi, V.A.; de Anda, F.; Gorbachev, A.Yu.; Vasil'ev, V.I. ; Smirnov, V.M.; Faleev, N.N.
Author Affiliation: IICO UASLP, San Luis Potosi, Mexico
Conference Title: Compound Semiconductors 1997. Proceedings of the IEEE Twenty-Fourth International Symposium on Compound Semiconductors p.37-40
Editor(s): Melloch, M.; Reed, M.A.
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xxvii+666 pp.
ISBN: 0 7503 0556 8 Material Identity Number: XX98-01948
U.S. Copyright Clearance Center Code: 0 7803 3883 9/98/$10.00
Conference Title: Compound Semiconductors 1997. Proceedings of the IEEE Twenty-Fourth International Symposium on Compound Semiconductors

Conference Date: 8-11 Sept. 1997 Conference Location: San Diego, CA, USA
Language: English
Abstract: We developed the LPE growth technology of InGaAsSb, AlGaAsSb and AlGaInAsSb layers from Sb-rich liquid phases on GaSb substrates. All multicomponent heterostructures were studied by double crystal X-ray diffraction. InGaAsSb layers were grown in both sides of the miscibility gap, near GaSb and near InAs. From a study of the variation of the rocking curves' halfwidth with the supercooling temperature of the **In-Ga-As-Sb** liquid phases the technological growth conditions were optimized. In the case of AlGaAsSb the GaSb substrate is eroded in contact with a saturated Al-**Ga-As-Sb** liquid due to the high non equilibrium degree on this system and the erosion increases with Al concentration. One of the techniques to diminish the erosion consists in increasing the initial supercooling but in this system, in the investigated area of compositions, it is impossible because of the low critical supercooling (Delta T/sub cr/) of the liquid phase. We have conceived and developed a method to control Delta T/sub cr/ by adding In to the Al-**Ga-As-Sb** liquid phase. It was found that when the In concentration increased the Delta T/sub cr/ also increased. So the transition from the quaternary AlGaAsSb to the pentanary AlGaInAsSb allowed us to decrease the erosion process. It is shown that high quality multicomponent Sb-based solid solutions can be grown by the developed technique with Sb as a solvent.
Subfile: A B

37/3,AB/12
DIALOG(R)File 2:INSPEC

6076828 INSPEC Abstract Number: A9824-7865-052, B9812-2520D-041
Title: Type II photoluminescence and conduction band offsets of **GaAsSb/InGaAs** and **GaAsSb** /InP heterostructures grown by metalorganic vapor phase epitaxy
Author(s): Hu, J.; Xu, X.G.; Stotz, J.A.H.; Watkins, S.P.; Curzon, A.E.; Thewalt, M.L.T.; Matine, N.; Bolognesi, C.R.
Author Affiliation: Dept. of Phys., Simon Fraser Univ., Burnaby, BC, Canada
Journal: Applied Physics Letters vol.73, no.19 p.2799-801
Publisher: AIP,
Publication Date: 9 Nov. 1998 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(19981109)73:19L.2799:TPCB;1-Q
Material Identity Number: A135-98046
U.S. Copyright Clearance Center Code: 0003-6951/98/73(19)/2799(3)/$15.00
Language: English
Abstract: The optical properties of lattice-matched **GaAsSb/** **InGaAs**/InP heterostructures with a varying **InGaAs** layer thickness (0-900 AA) were investigated. These structures display strong low temperature type II luminescence, the energy of which varies with the **InGaAs** layer thickness and ranges from 0.453 to 0.63 eV. The type II luminescence was used to determine directly and accurately the conduction band offset of these structures. The values obtained herein are 0.36 and 0.18 eV at 4.2 K for the **GaAsSb/InGaAs** and **GaAsSb**/InP **heterojunctions**, respectively, with the **GaAsSb** conduction band higher in energy.
Subfile: A B

37/3,AB/13
DIALOG(R)File 2:INSPEC

5730814 INSPEC Abstract Number: B9712-2560J-001
Title: Oxide defined AlAsSb/**InGaAs**/InP **heterojunction** bipolar transistors with a buried metal extrinsic base
Author(s): Lear, K.L.; Blum, O.; Klem, J.F.
Author Affiliation: Sandia Nat. Labs., Albuquerque, NM, USA
Conference Title: 1997 55th Annual Device Research Conference Digest (Cat. No.97TH8279) p.66-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 175 pp.
ISBN: 0 7803 3911 8 Material Identity Number: XX97-01981
Conference Title: 1997 55th Annual Device Research Conference Digest
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 23-25 June 1997 Conference Location: Fort Collins, CO, USA
Language: English
Abstract: Wet thermal oxidation of aluminum containing III-V semiconductors is a potent alternative technique for fabricating optoelectronic and microelectronic devices. Oxides have previously been used to define emitter openings of AlGaAs **heterojunction** bipolar transistors (**HBTs**) in low capacitance collector-up configurations. In the present work, the unique metal formation of AlAsSb oxidation is used to reduce the extrinsic base resistance under the collector in **HBTs** on InP. In particular, oxidation of AlAsSb can produce an insulating alumina film with a self-aligned, adjacent elemental antimony layer. We report on the electrical properties of this metal layer and the demonstration of **HBTs** with embedded metal underlying the extrinsic base. The combined low resistance and capacitance of such structures can potentially yield higher speed operation.
Subfile: B

37/3,AB/14
DIALOG(R)File 2:INSPEC

5593674 INSPEC Abstract Number: A9713-8115G-021, B9707-0510D-055
Title: Epitaxy and properties of InMnAs/AlGaSb diluted magnetic III-V semiconductor heterostructures
Author(s): Shen, A.; Matsukura, F.; Sugawara, Y.; Kuroiwa, T.; Ohno, H.; Oiwa, A.; Endo, A.; Katsumoto, S.; Iye, Y.
Author Affiliation: Res. Inst. of Electr. Commun., Tohoku Univ., Sendai, Japan
Journal: Applied Surface Science Conference Title: Appl. Surf. Sci. (Netherlands) vol.113-114 p.183-8
Publisher: Elsevier,
Publication Date: April 1997 Country of Publication: Netherlands
CODEN: ASUSEE ISSN: 0169-4332
SICI: 0169-4332(199704)113/114L.183:EPIA;1-L
Material Identity Number: I974-97008
U.S. Copyright Clearance Center Code: 0169-4332/97/$17.00
Conference Title: ICSFS-8. Eighth International Conference on Solid Films

and Surfaces
Conference Sponsor: Japan Soc. Promotion of Sci
Conference Date: 1-5 July 1996 Conference Location: Osaka, Japan
Language: English
Abstract: InMnAs/AlGaSb diluted magnetic semiconductor heterostructures have been grown by molecular-beam epitaxy on **GaAs** substrates. Three epitaxial procedures were employed for the growth of InMnAs, which resulted in three-dimensional or two-dimensional nucleation. Low-temperature magnetotransport measurements reveal that while some of the samples show well-aligned ferromagnetic ordering some others show ferromagnetic behavior with no magnetic anisotropy or, in the extreme case, superparamagnetic behavior. The transport properties were correlated to the growth modes.
Subfile: A B

37/3,AB/15
DIALOG(R)File 2:INSPEC

5587235 INSPEC Abstract Number: A9713-7340L-004, B9707-2530C-006
Title: Increased electron concentration in InAs/AlGaSb heterostructures using a Si planar doped ultrathin InAs quantum well
Author(s): Sasa, S.; Yamamoto, Y.; Izumiya, S.; Yano, M.; Iwai, Y.; Inoue, M.
Author Affiliation: Dept. of Electr. Eng., Osaka Inst. of Technol., Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) Conference Title: Jpn. J. Appl. Phys. 1, Regul. Pap. Short Notes Rev. Pap. (Japan) vol.36, no.3B p.1869-71
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: March 1997 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(199703)36:3BL.1869:IECI;1-Y
Material Identity Number: F221-97007
Conference Title: 1996 International Conference on Solid State Devices and Materials (SSDM'96)
Conference Date: 26-29 Aug. 1996 Conference Location: Yokohama, Japan
Language: English
Abstract: We demonstrate that the two-dimensional electron gas concentration in an InAs/AlGaSb heterostructure can be greatly increased by introducing a Si planar-doped ultrathin InAs quantum well (QW) sandwiched between AlSb barriers as an additional electron supplying layer in a well controlled fashion. With the Si planar-doped QW formed 8 nm below the channel layer, the sheet electron concentration increased up to 4.5*10/sup 12/ cm/sup -2/ with an electron mobility of 4*10/sup 4/ cm/sup 2//Vs at 77 K. Shubnikov-de Haas measurements revealed that only two subbands are occupied, even for heavily doped samples. The energy separation between the first and the second subbands is as large as 100 meV, indicating a strong electron confinement in the selectively doped InAs/AlGaSb heterostructures.
Subfile: A B

37/3,AB/16
DIALOG(R)File 2:INSPEC

5410082 INSPEC Abstract Number: A9623-6590-001
Title: Determination of the thermal properties of semiconductors using the

photothermal method in the many thin layers case
Author(s): Saadallah, F.; Yacoubi, N.; Hfaiedh, A.
Author Affiliation: IPEIN, Nabeul, Tunisia
Journal: Optical Materials Conference Title: Opt. Mater. (Netherlands) vol.6, no.1-2 p.35-9
Publisher: Elsevier,
Publication Date: July 1996 Country of Publication: Netherlands
CODEN: OMATET ISSN: 0925-3467
SICI: 0925-3467(199607)6:1/2L.35:DTPS;1-S
Material Identity Number: N662-96004
U.S. Copyright Clearance Center Code: 0925-3467/96/$15.00
Conference Title: Materials for Optoelectronics
Conference Date: 22-23 Aug. 1995 Conference Location: Sheffield, UK
Language: English
Abstract: The photothermal method has been used in order to determine the thermal properties of semiconductors. In this work, a simple expression for the periodic temperature, at the sample's surface, which is valuable for a number of layers deposited on a substrate, was introduced. This expression showed a very good agreement with data obtained using the **GaAsSb**/ **GaAs** and InP/GaInAs/InP heterostructures, when the sum of the thicknesses of all the layers is much smaller than the thickness of the substrate. This condition is often satisfied when dealing with semiconductors used in microoptoelectronics.
Subfile: A

? T S37/3,AB/17-29

37/3,AB/17
DIALOG(R)File 2:INSPEC

5219806 INSPEC Abstract Number: B9605-0510D-078
Title: Growth and doping of **GaAsSb** via metalorganic chemical vapor deposition for InP **heterojunction** bipolar transistors
Author(s): McDermott, B.T.; Gertner, E.R.; Pittman, S.; Seabury, C.W.; Chang, M.F.
Author Affiliation: Sci. Center, Rockwell Int. Corp., Thousand Oaks, CA, USA
Journal: Applied Physics Letters vol.68, no.10 p.1386-8
Publisher: AIP,
Publication Date: 4 March 1996 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(19960304)68:10L.1386:GDGM;1-7
Material Identity Number: A135-96011
U.S. Copyright Clearance Center Code: 0003-6951/96/68(10)/1386/3/$10.00
Language: English
Abstract: **GaAsSb** is a low band gap, lattice matched to InP, alternative to GaInAs. Growth and doping using diethyltellurium and carbon tetrachloride were investigated. Hole concentrations up to 1.3*10/sup 20/ cm/sup -3/ have been achieved in as-grown carbon-doped **GaAsSb** [i.e., no postgrowth annealing was necessary for dopant activation, a key requirement for n-p-n **heterojunction** bipolar transistor (**HBT**) structures]. This is a sevenfold improvement over the best carbon-doped **InGaAs** reported by metalorganic chemical vapor deposition. Hall measurements indicate that **GaAsSb** `s hole mobility is 55%-60% of GaInAs`s, for a given carrier concentration. InP **HBTs** with carbon-doped **GaAsSb** base are demonstrated.
Subfile: B

37/3,AB/18
DIALOG(R)File 2:INSPEC

5195545 INSPEC Abstract Number: B9604-2560J-012
Title: InP/**GaAsSb**/InP and InP/**GaAsSb**/InGaAsP double **heterojunction** bipolar transistors with a carbon-doped base grown by organometallic chemical vapor deposition
Author(s): Bhat, R.; Hong, W.-P.; Caneau, C.; Koza, M.A.; Nguyen, C.-K.; Goswami, S.
Author Affiliation: Bellcore, Red Bank, NJ, USA
Journal: Applied Physics Letters vol.68, no.7 p.985-7
Publisher: AIP,
Publication Date: 12 Feb. 1996 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(19960212)68:7L.985:GGID;1-P
Material Identity Number: A135-96008
U.S. Copyright Clearance Center Code: 0003-6951/96/68(7)/985/3/$10.00
Language: English
Abstract: InP/**GaAsSb** double **heterojunction** bipolar transistors (DHBTs) may be an attractive alternative to InP/**InGaAs** DHBTs, since estimates of the band alignment indicate that it is ideal for fabricating n-p-n DHBTs. We have demonstrated the first organometallic chemical vapor deposition grown InP/**GaAsSb** DHBTs, with carbon-doped bases having an f/sub t/ and f/sub max/ of 30 and 45 GHz, respectively.
Subfile: B

37/3,AB/19
DIALOG(R)File 2:INSPEC

5189074 INSPEC Abstract Number: A9606-8630J-056, B9603-8420-293
Title: **GaAsSb**-based **heterojunction** tunnel diodes for tandem solar cell interconnects
Author(s): Zolper, J.C.; Klem, J.F.; Plut, T.A.; Tigges, C.P.
Author Affiliation: Sandia Nat. Labs., Albuquerque, NM, USA
Conference Title: 1994 IEEE First World Conference on Photovoltaic Energy Conversion. Conference Record of the Twenty Fourth IEEE Photovoltaic Specialists Conference-1994 (Cat.No.94CH3365-4) Part vol.2 p.1843-6 vol.2
Publisher: IEEE, New York, NY, USA
Publication Date: 1994 Country of Publication: USA 2 vol. 2402 pp.
ISBN: 0 7803 1460 3 Material Identity Number: XX95-02435
U.S. Copyright Clearance Center Code: CH3365-4/94/0000-1843$4.00
Conference Title: Proceedings of 1994 IEEE 1st World Conference on Photovoltaic Energy Conversion - WCPEC (A Joint Conference of PVSC, PVSEC and PSEC)
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 5-9 Dec. 1994 Conference Location: Waikoloa, HI, USA
Language: English
Abstract: We report a new approach to tunnel junctions that employs a pseudomorphic **GaAsSb** layer to obtain a band alignment at a **InGaAs** or InAlAs p-n junction favorable for forward bias tunneling. Since the majority of the band offset between **GaAsSb** and **InGaAs**

or InAlAs is in the valence band, when an **GaAsSb** layer is placed at an **InGaAs** or InAlAs p-n junction the tunneling distance is reduced and the tunneling current is increased. For all doping levels studied, the presence of the **GaAsSb** -layer enhanced the forward tunneling characteristics. In fact, in a **InGaAs/GaAsSb** tunnel diode with p=1.5*10/sup 18/ cm/sup -3/ a peak tunneling current sufficient for a 1000 sun InP/**InGaAs** tandem solar cell interconnect was achieved while a similarly doped all-**InGaAs** diode was rectifying. This approach affords a new degree of freedom in designing tunnel junctions for tandem solar cell interconnects. Previously only doping levels could be varied to control the tunneling properties. Our approach relaxes the doping requirements by employing a **GaAsSb**-based **heterojunction**.
Subfile: A B

37/3,AB/20
DIALOG(R)File 2:INSPEC

5180228 INSPEC Abstract Number: A9605-4260B-027, B9603-4320J-138
Title: A novel pseudomorphic (**GaAs**/sub 1-x/Sb/sub x/-In/sub y/Ga/sub 1-y/As)/**GaAs** bilayer-quantum-well structure lattice-matched to **GaAs** for long-wavelength optoelectronics
Author(s): Peter, M.; Forker, J.; Winkler, K.; Bachem, K.H.; Wagner, J.
Author Affiliation: Fraunhofer-Inst. fur Angewandte Festkorperphys., Freiburg, Germany
Journal: Journal of Electronic Materials Conference Title: J. Electron. Mater. (USA) vol.24, no.11 p.1551-5
Publisher: TMS,
Publication Date: Nov. 1995 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
SICI: 0361-5235(199511)24:11L.1551:NPGX;1-B
Material Identity Number: J246-96002
Conference Title: 7th Biennial Workshop on Organometallic Vapor Phase Epitaxy
Conference Date: 2-6 April 1995 Conference Location: Fort Meyers, FL, USA
Language: English
Abstract: Two types of quantum well (QW) structures grown lattice matched on (100) **GaAs** have been studied. The first type of structure consists of pseudomorphic **GaAs**/sub x/Sb/sub 1-x//**GaAs** (x<or=0.3) SQWs which show emission wavelengths longer than those reported for pseudomorphic In/sub y/Ga/sub 1-y/As/**GaAs** QWs. However, the attractive emission wavelength of 1.3 mu m has not been achieved. To reach this goal, a novel type of bilayer QW (BQW) has been grown consisting of a stack of two adjacent pseudomorphic layers of **GaAs**/sub x/Sb/sub 1-x/ and In/sub x/Ga/sub 1-y/As embedded between **GaAs** confinement layers. In this BQW, a type-II **heterojunction** is formed between **GaAs** /sub x/Sb/sub 1-x/ and In/sub y/Ga/sub 1-y/As, resulting in a spatially indirect radiative recombination of electrons and holes at emission wavelengths longer than those achieved in the **GaAs**/sub x/Sb/sub 1-x// **GaAs** and In/sub y/Ga/sub 1-y/As/**GaAs** SQWs. The longest 300 K emission wavelength observed so far was 1.332 mu m.
Subfile: A B

37/3,AB/21

DIALOG(R)File 2:INSPEC

5143666 INSPEC Abstract Number: B9602-2560R-014
Title: Rapid thermal annealing effects on the structural integrity of InAlAs/**GaAsSb** HIGFET epilayers on InP
Author(s): Merkel, K.G.; Cerny, C.L.A.; Lareau, R.T.; Bright, V.M.; Yu, P.W.; Schuermeyer, F.L.
Author Affiliation: Dept. of Electr. & Comput. Eng., Air Force Inst. of Technol., Wright-Patterson AFB, OH, USA
Conference Title: Compound Semiconductors 1994. Proceedings of the Twenty-First International Symposium p.727-32
Editor(s): Goronkin, H.; Mishra, U.
Publisher: IOP Publishing, Bristol, UK
Publication Date: 1995 Country of Publication: UK xxvii+912 pp.
ISBN: 0 7503 0226 7
Conference Title: Proceedings of the Twenty-First International Symposium on Compound Semiconductors
Conference Sponsor: Motorola; Office of Naval Res.; ARPA; Siemens, EPI; EMCORE; Bellcore; et al
Conference Date: 18-22 Sept. 1994 Conference Location: San Diego, CA, USA
Language: English
Abstract: The upper thermal limit for In/sub 0.52/Al/sub 0.48/As/ **GaAs**/sub 0.51/Sb/sub 0.49/ **heterojunction** insulated-gate FET (HIGFET) epilayers is determined for both self-aligned gate (SAG) and recessed gate (RG) designs. Photoluminescence (PL), secondary ion mass spectroscopy (SIMS) and Auger electron spectroscopy (AES) are used to monitor degradation following rapid thermal annealing (RTA) at temperatures between 600 and 800 degrees C. Epilayer integrity is maintained in both the SAG and RG structures to 600 degrees C. Interfacial degradation following RTA at 700 degrees C is more severe for the SAG structure. After 800 degrees C RTA, the **GaAs** /sub 0.51/Sb/sub 0.49/ channel no longer exists in either sample due to Ga and Sb indiffusion, and In and Al outdiffusion to the sample surface. The SIMS and AES results correlate with the PL results and indicate rapid thermal processing temperature limits of 500 degrees C for the SAG HIGFET and 700 degrees C for the RG HIGFET.
Subfile: B
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37/3,AB/22
DIALOG(R)File 2:INSPEC

4454737 INSPEC Abstract Number: A9317-7320-040, B9309-2530B-008
Title: Measurement of valence band edge discontinuity for the InAlAs/ **GaAsSb heterojunction** lattice-matched to InP
Author(s): Martinez, M.J.; Scherer, R.L.; Schuermeyer, F.L.; Johnstone, D.K.; Stutz, C.E.; Evans, K.R.
Author Affiliation: Wright Lab., Wright-Patterson AFB, OH, USA
Conference Title: Fourth International Conference on Indium Phosphide and Related Materials (Cat. No.92CH3104-7) p.354-6
Publisher: IEEE, New York, NY, USA
Publication Date: 1992 Country of Publication: USA xx+687 pp.
ISBN: 0 7803 0522 1
Conference Sponsor: IEEE
Conference Date: 21-24 April 1992 Conference Location: Newport, RI, USA

Language: English
Abstract: The authors describe the measurement of the valence band-edge discontinuity in InAlAs/**GaAsSb** lattice-matched to InP using the activation energy of a single barrier diode constructed of these materials. It is shown that, near room temperature, the current exhibits an exponential dependence on the inverse temperature, and the activation energy of this behavior is not strongly dependent on any parameter of the system except the band-edge discontinuity. It is further shown that, for small applied voltages, the activation energies have a linear dependence on this voltage which can be extrapolated to an equilibrium value for no applied voltage. The calculated equilibrium value of 640 meV+or-20 meV agrees well with modeled values and with experimentally observed trends. It is therefore believed that this result can be used with a high degree of confidence by device designers and that it demonstrates the great potential of the **heterojunction** for use in advanced device design.
Subfile: A B

37/3,AB/23
DIALOG(R)File 2:INSPEC

04360810 INSPEC Abstract Number: B9304-2560J-021
Title: High gain AlInAs/**GaAsSb**/AlInAs NpN **HBTs** on InP
Author(s): Sullivan, G.J.; Farley, C.W.; Ho, W.J.; Pierson, R.L.; Szwed, M.K.; Lind, M.D.; Bernescut, R.L.
Author Affiliation: Rockwell Int. Sci. Center, Thousand Oaks, CA, USA
Journal: Journal of Electronic Materials vol.21, no.12 p.1123-5
Publication Date: Dec. 1992 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
U.S. Copyright Clearance Center Code: 0361-5235/92/1401-1123$5.00
Language: English
Abstract: The authors report the first growth and characterization of high gain double **heterojunction** NpN **HBTs** on InP with a lattice-matched **GaAs**/sub .5/Sb/sub .5/ base layer. This AlInAs/ **GaAsSb** **heterojunction** has almost no discontinuity in the conduction band edge, eliminating the need to grade the emitter-to-base **heterojunction** to achieve optimal carrier injection. The layers were grown in a solid source MBE system, using tetramer As/sub 4/ and Sb/sub 4/ sources. Be is an efficient acceptor in the **GaAsSb**, but the mobility is about half that measured in p type **GaAs** on **GaAs** substrates. The **HBTs** fabricated were large area mesa isolated transistors, with a beta of 80 at a current density of 2 kA/cm/sup 2/, and the gain remained high at lower current densities. The turnon voltage, V/sub be/, is only 0.45 V at a current density of 2 A/cm/sup 2/.
Subfile: B

37/3,AB/24
DIALOG(R)File 2:INSPEC

04162090 INSPEC Abstract Number: A9213-6855-049
Title: Incorporation rate variation at heterointerfaces during III-V molecular beam epitaxy
Author(s): Evans, K.R.; Stutz, C.E.; Taylor, E.N.; Ehret, J.E.
Author Affiliation: Wright Lab., Wright-Patterson AFB, OH, USA
Journal: Applied Surface Science vol.56-58, no.1-4, pt.B p.677-83
Publication Date: March 1992 Country of Publication: Netherlands

CODEN: ASUSEE ISSN: 0169-4332
U.S. Copyright Clearance Center Code: 0169-4332/92/$05.00
Conference Title: 3rd International Conference on the Formation of Semiconductor Interfaces. ICFSI-3
Conference Date: 6-10 May 1991 Conference Location: Rome, Italy
Language: English

Abstract: Surface composition is known to influence cation and anion incorporation rates (IRs) during III-V molecular beam epitaxy (MBE) at high growth temperatures. Consequently, IRs can vary at heterointerfaces. The present study examines the temporal behavior of IRs during formation of AlGaAs/**GaAs**, GaInAs/**GaAs** and **GaAsSb/GaAs** heterointerfaces. Incorporation rates are deduced from the in situ detection via desorption mass spectrometry of the non-incorporated. or desorbed, fraction of the incident beam. Predicted compositional profiles are calculated from the observed IR variations and show significant enrichment in composition of one of the constituent species at the heterointerface. The predicted compositional profile for the GaInAs/ **GaAs** system is qualitatively verified by X-ray diffraction and photoluminescence measurements on separately grown structures. These results are interpreted on the basis of simple first-order desorption considerations which incorporate strain-dependent activation energies for desorption.
Subfile: A

37/3,AB/25
DIALOG(R)File 2:INSPEC

03555077 INSPEC Abstract Number: A90028618
Title: Electrical characteristics and energy-band offsets in nInAs/sub 0.89/Sb/sub 0.11//n-GaSb **heterojunctions** grown by the liquid phase epitaxy technique
Author(s): Mebarki, M.; Kadri, A.; Mani, H.
Author Affiliation: Dept. of Phys., Univ. of Oran-Es-Senia, Algeria
Journal: Solid State Communications vol.72, no.8 p.795-8
Publication Date: Nov. 1989 Country of Publication: USA
CODEN: SSCOA4 ISSN: 0038-1098
U.S. Copyright Clearance Center Code: 0038-1098/89/$3.00+.00
Language: English
Abstract: Liquid-phase-epitaxy (LPE) grown **heterojunctions** of n-type inAs/sub 0.89/Sb/sub 0.11/ lattice-matched to n-type Te-doped GaSb(100) substrates, were studied by capacitance-voltage measurements at T=77 K. By using the electric displacement continuity, it is shown that the band-lineup of this material is of the broken type with conduction-band and valence-band offsets Delta E/sub c/=0.82 eV and Delta E/sub nu /=0.36. The electron affinity of InAs/sub 0.89/Sb/sub 0.11/ alloy is also determined to be X=4.87 eV.
Subfile: A

37/3,AB/26
DIALOG(R)File 2:INSPEC

02880995 INSPEC Abstract Number: B87032486
Title: An (Al,**Ga)As/GaAs** heterostructure bipolar transistor with nonalloyed graded-gap ohmic contacts to the base and emitter

Author(s): Rao, M.A.; Caine, E.J.; Long, S.I.; Kroemer, H.
Author Affiliation: Dept. of Electr. & Comput. Eng., California Univ., Santa Barbara, CA, USA
Journal: IEEE Electron Device Letters vol.EDL-8, no.1 p.30-2
Publication Date: Jan. 1987 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/87/0100-0030$01.00
Language: English
Abstract: Graded regions of n-(**Ga**,**In**)**As** and p-**Ga**(**As**,**Sb**) were incorporated side-by-side as emitter and base contacts, respectively, into an n-p-n (Al,**Ga**)**As**/**GaAs** heterostructure bipolar transistor (**HBT**). The process involved two separate molecular beam epitaxy (MBE) growths, leading to base contact regions that were self-aligned to the emitter mesas. The devices could be easily probed with pressure contacts even prior to any metallization, and excellent characteristics were obtained after final metallization. Contact resistivities of 5*10/sup -7/ and 3*10/sup -6/ Omega *cm/sup 2/ were measured for n- and p-type graded-gap ohmic contact structures, respectively.
Subfile: B

37/3,AB/27
DIALOG(R)File 2:INSPEC

01278934 INSPEC Abstract Number: A78095348, B79000724
Title: Superfine heterostructures of In/sub 1-x/Ga/sub x/As and GaSb/sub 1-y/As/sub y/
Author(s): Chang, L.L.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Journal: Journal of Vacuum Science and Technology vol.15, no.4 p. 1478-9
Publication Date: July-Aug. 1978 Country of Publication: USA
CODEN: JVSTAL ISSN: 0022-5355
Conference Title: Proceedings of the 5th Annual Conference on the Physics of Compound Semiconductor Interfaces
Conference Sponsor: American Vacuum Soc., Office Naval Res
Conference Date: 17-20 Jan. 1978 Conference Location: Los Angeles, CA, USA
Language: English
Abstract: Summary form only given, substantially as follows. The system offers the rather unique feature that, by varying the alloy compositions of x and y independently, the conduction bandedge of In/sub 1-x/Ga/sub x/As can be controlled to be close to, and may lie either above or below the valence bandedge of GaSb/sub 1-y/As/sub y/, and yet their lattice constants can be simultaneously matched. The deposition was carried out on (100) InAs, GaSb, and **GaAs** substrates kept at a relatively low temperature of 450 degrees -600 degrees C, using elemental sources of the constituents, **In**, **Ga**, **As**, and **Sb**. Impurity sources of Sn or Te were incorporated to give the desirable carrier concentrations. The growth was monitored by high-energy electron diffraction which, for smoothed-out surfaces, showed streaked patterns with fractional orders as a result of reconstruction. A variety of patterns were observed: The common ones under typical growth conditions of excessive vapor beams of the group V elements were c(2*8) for In/sub 1-x/Ga/sub x/As over the entire composition range, and c(2*6) for y<or approximately=0.2 and c(2*8) for y>or approximately=0.5 with a transitional region between the limits for GaSb/sub 1-y/As/sub y/.

At the start of heteroepitaxy, the streaked pattern characteristic of one material changed instantaneously to that of the other as long as the lattice mismatch was smaller than about 2.5%, while an intervening nucleation step occurred otherwise.
Subfile: A B

37/3,AB/28
DIALOG(R)File 2:INSPEC

01047932 INSPEC Abstract Number: A77038894, B77017473
Title: Diode sources for 1.0 to 1.2 mu m emission
Author(s): Nuese, C.J.
Author Affiliation: RCA Labs., Princeton, NJ, USA
Conference Title: International Electron Devices Meeting. (Technical digest) p.125-8
Publisher: IEEE, New York, NY, USA
Publication Date: 1976 Country of Publication: USA xiv+669+15 (suppl.) pp.
Conference Sponsor: IEEE
Conference Date: 6-8 Dec. 1976 Conference Location: Washington, DC, USA
Language: English
Abstract: The properties of silica fibers that are potentially attractive for fiber-optic systems at wavelengths between about 1.0 and 1.2 mu m are considered. The features and deficiencies of semiconductor LEDs and lasers that could be used in this wavelength range are then reviewed and compared. These sources include: Si-compensated LEDs of **GaAs** and InP: ternary homojunctions of **(In,Ga)As**, **In(As**,P), and **Ga(As,Sb**); 'pseudo' III-Vs or II-VIs such as CuInSe/sub 2/ and CdSnP/sub 2/; and **heterojunction** lasers and LEDs of **(In, Ga)As**/**(In,Ga)**P, **Ga(As,Sb)**/(Al, **Ga)(As,Sb)**, and **(In,Ga)(As**,P)/InP.
Subfile: A B

37/3,AB/29
DIALOG(R)File 2:INSPEC

00472846 INSPEC Abstract Number: A73002682, B73004953
Title: III-V crystalline solid solution systems
Author(s): Panish, M.B.; Ilegems, M.
Author Affiliation: Bell Telephone Labs., Murray Hill, NJ, USA
Conference Title: Proceedings of the Third International Symposium on Gallium Arsenide and Related Compounds p.67-79
Editor(s): Paulus, K.
Publisher: Inst. Phys, London, UK
Publication Date: 1971 Country of Publication: UK ix+297 pp.
Conference Sponsor: Inst. Phys.; United States Air Force
Conference Date: 5-7 Oct. 1970 Conference Location: Aachen, West Germany
Language: English
Abstract: There is an increasing interest in the crystalline solid solution III-V systems for spontaneous light-emitting diodes and because several of these systems with close lattice matching properties will permit the preparation of essentially clean **heterojunctions** and the devices which result therefrom. Work with these systems results in rather different

metallurgical problems than are ordinarily encountered with binary compound semiconductors or elemental semiconductors. These problems arise primarily from the more complicated phase equilibria and because of lattice mismatch. Methods for the calculation of III-V ternary phase diagrams are discussed and illustrated with the Ga-In-P, Al-Ga-P and Al-In-P systems. Lattice matching conditions on isotherms in two quarternary systems, Al-Ga-**In**
-P and **Ga-Sb-In-As** are discussed, and one
quaternary system consisting of a dopant Sn, plus a presently useful ternary Al-**Ga-As** is discussed.

Subfile: A B

47/3,AB/1
DIALOG(R)File 2:INSPEC

5294998 INSPEC Abstract Number: A9614-8115G-018, B9607-0510D-119
Title: MOVPE growth of Ill-V compounds for optoelectronic and electronic applications
Author(s): Behet, M.; Hovel, R.; Kohl, A.; Mesquida, A.; Kusters, M.A.; Opitz, B.; Heime, K.
Author Affiliation: Inst. fur Halbleitertechnik, Tech. Hochschule Aachen, Germany
Journal: Microelectronics Journal vol.27, no.4-5 p.297-334
Publisher: Elsevier,
Publication Date: July-Aug. 1996 Country of Publication: UK
CODEN: MICEB9 ISSN: 0026-2692
SICI: 0026-2692(199607/08)27:4/5L.297:MGCO;1-5
Material Identity Number: M243-96004
U.S. Copyright Clearance Center Code: 0026-2692/96/$15.00
Language: English
Abstract: This paper reviews some of the most important aspects of MOVPE of III-V semiconductors. The paper starts with fundamental aspects of MOVPE in general, and turns to the use of novel precursors and precursor combinations with special emphasis on improvements in safety, material consumption, reactivities or precursor combinations and layer purity. The next section discusses special problems and advantages of selective area growth and growth on patterned substrates. Then the growth of heterostructures, quantum wells and superlattices for field-effect transistors, Wannier-Stark modulators and resonant tunnelling diodes is described. It will be shown that different growth parameters, e.g. different switching sequences between individual layers, are needed for either optoelectronic or electronic devices. The usefulness of MOVPE for various material combinations such as AlGaAs/**GaAs**, InP/**InGaAs**, **InGaAs**/**InGaAs** , InGaAsP/InGaAsP, InAs/AlSb and InAs/InPSb will be demonstrated by material properties and device performances.
Subfile: A B

? T S43/3,AB/1-11

43/3,AB/1
DIALOG(R)File 2:INSPEC

6215774 INSPEC Abstract Number: B1999-05-2560R-053
Title: Application of a new airbridge-gate structure for high-performance Ga/sub 0.51/In/sub 0.49/P/In/sub 0.15/Ga/sub 0.85/As/**GaAs** pseudomorphic field-effect transistors
Author(s): Wen-Chau Liu; Wen-Lung Chang; Hsi-Jen Pan; Kuo-Hui Yu; Shung-Ching Feng; Wen-Shiung Lour
Author Affiliation: Dept. of Electr. Eng., Nat. Cheng Kung Univ., Tainan, Taiwan
Journal: Applied Physics Letters vol.74, no.14 p.1996-8
Publisher: AIP,
Publication Date: 5 April 1999 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(19990405)74:14L.1996:AAGS;1-E
Material Identity Number: A135-1999-013
U.S. Copyright Clearance Center Code: 0003-6951/99/74(14)/1996(3)/$15.00
Language: English
Abstract: A new high-performance Ga/sub 0.51/In/sub 0.49/P/In/sub 0.15/Ga/sub 0.85/As/**GaAs** pseudomorphic heterostructure field-effect transistor, based on a novel airbridge-gate structure with multiple piers, has been fabricated successfully. Due to the employment of high Schottky **barrier** GaInP **layer** and the newly designed double delta-doped sheets (D/sup 3/S) **InGaAs** channel, the high gate-to-drain breakdown voltage and broad and linear transconductance are obtained simultaneously. Moreover, the use of airbridge-gate technique not only suppresses the parasitic capacitance, but also exhibits a wide and flat operation regime of the current gain cutoff frequency f/sub T/ and maximum oscillation frequency f/sub max/.
Subfile: B

43/3,AB/2
DIALOG(R)File 2:INSPEC

6208236 INSPEC Abstract Number: A1999-09-7360L-019, B1999-05-2560S-008
Title: Characteristics of electron traps in Si-doped Ga/sub 0.51/In/sub 0.49/P and electrical properties of modulation doped GaInP/**InGaAs**/**GaAs** heterostructures
Author(s): Besikci, C.; Civan, Y.
Author Affiliation: Dept. of Electr. Eng., Middle East Tech. Univ., Ankara, Turkey
Journal: Thin Solid Films vol.338, no.1-2 p.213-19
Publisher: Elsevier,
Publication Date: 29 Jan. 1999 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
SICI: 0040-6090(19990129)338:1/2L.213:CETD;1-A
Material Identity Number: T070-1999-006
U.S. Copyright Clearance Center Code: 0040-6090/99/$20.00
Language: English
Abstract: In order to investigate the feasibility of Si-doped Ga/sub 0.51/In/sub 0.49/P for modulation-doped field effect transistor

applications, single Ga/sub 0.51/In/sub 0.49/P layers and Ga/sub 0.51/In/sub 0.49/P/In/sub x/Ga/sub 1-x/As/**GaAs** (x=0,0.15 and 0.25) modulation doped heterostructures grown by gas source molecular beam epitaxy were characterized through deep level transient spectroscopy and Hall-effect measurements. Electrical characterization of the undoped and moderately Si-doped (N/sub D/=3*10/sup 17/ cm/sup -3/) GaInP layers yielded an electron trap with an activation energy of 0.75 eV and a temperature dependent capture cross section with a capture barrier of 0.593 eV. The density of this trap increased, and an anomalous decrease in the free carrier concentration of GaInP was observed after the samples were annealed at temperatures typically used in device processing. While, this trap showed characteristics similar to DX centers, it was not detected in highly Si doped (N/sub D/ approximately=4*10/sup 18/ cm/sup -3/) as grown layers suggesting that the trap is a defect complex including a residual impurity. While very high two-dimensional electron gas density (2.6*10/sup 12/ cm/sup -2/ at 30 K) was achieved in the lattice matched (x=0) structures, the strained structures were found to be very sensitive to heat treatment, although the **InGaAs** layers thicknesses were below the theoretical critical thickness. Persistent photoconductivity and a significant reduction in the interface sheet electron density were observed after annealing. The anomalous behavior can be attributed to the decrease in the carrier concentration of the doped GaInP **barrier layer** and to the strain relaxation at the hetero-interface after annealing. While other explanations may be possible, the decrease in the GaInP electron concentration can be attributed to Si atoms moving from donor to acceptor sites.

Subfile: A B

43/3,AB/3

DIALOG(R)File 2:INSPEC

6188760 INSPEC Abstract Number: A1999-08-4255P-020, B1999-04-4320J-158

Title: Effects of an InGaP electron **barrier layer** on 1.55 mu m laser diode performance

Author(s): Abraham, P.; Piprek, J.; DenBaars, S.P.; Bowers, J.E.

Author Affiliation: Dept. of Electron. & Comput. Eng., California Univ., Santa Barbara, CA, USA

Conference Title: Conference Proceedings. 1998 International Conference on Indium Phosphide and Related Materials (Cat. No.98CH36129) p.713-16

Publisher: IEEE, New York, NY, USA

Publication Date: 1998 Country of Publication: USA xvi+849 pp.

ISBN: 0 7803 4220 8 Material Identity Number: XX-1998-02173

U.S. Copyright Clearance Center Code: 0 7803 4220 8/98/$10.00

Conference Title: Conference Proceedings. 1998 International Conference on Indium Phosphide and Related Materials

Conference Sponsor: Japan Soc. Appl. Phys.; IEEE/Lasers & Electro-Opt. Soc.; IEEE Electron Devices Soc.; Univ. Tsukuba; IEICE of Japan; Optoelectron. Ind. & Technol. Dev. Assoc.; Res. & Dev. Assoc.; Res. & Dev. Assoc. Future Electron Devices

Conference Date: 11-15 May 1998 Conference Location: Tsukuba, Japan

Language: English

Abstract: Temperature sensitive loss mechanisms are known to severely limit the performance of InGaAsP/InP laser diodes emitting at 1.55 mu m. In this paper, we report on a simple modification of the classical InGaAsP laser structure to reduce electron leakage from the separate **confinement** heterostructure (SCH) **layer**.

Subfile: A B

43/3,AB/4
DIALOG(R)File 2:INSPEC

6090868 INSPEC Abstract Number: B9901-2530B-009
Title: Low temperature growth and characterization of silicon delta doped GaInP/GaInAs/**GaAs** pseudomorphic heterostructures for use in high electron mobility transistors
Author(s): Smart, J.A.; Chumbes, E.M.; Eastman, L.F.; Shealy, J.R.
Author Affiliation: OMVPE Fac., Cornell Univ., Ithaca, NY, USA
Conference Title: Compound Semiconductors 1997. Proceedings of the IEEE Twenty-Fourth International Symposium on Compound Semiconductors p.91-4
Editor(s): Melloch, M.; Reed, M.A.
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xxvii+666 pp.
ISBN: 0 7503 0556 8 Material Identity Number: XX98-01948
U.S. Copyright Clearance Center Code: 0 7803 3883 9/98/$10.00
Conference Title: Compound Semiconductors 1997. Proceedings of the IEEE Twenty-Fourth International Symposium on Compound Semiconductors
Conference Date: 8-11 Sept. 1997 Conference Location: San Diego, CA, USA
Language: English
Abstract: Flow modulation organometallic vapor phase epitaxy (OMVPE) was used to synthesize selectively doped GaInP/GaInAs/**GaAs** pseudomorphic heterostructures. Transport properties of the two dimensional electron gas (2DEG) were optimized with various buffer formation schemes, techniques for single sided doping, and the **channel** and spacer **layer** thicknesses. **GaAs** buffers were deposited at 550 degrees C and 635 degrees C, while GaInP layers were grown at 550 degrees C to promote atomic disordering. Achieving high 2DEG densities involved incorporating several delta doping supply layers separated by thin GaInP regions. Mobilities as high as 5100 cm/sup 2/ volt/sup -1/ sec/sup -1/ with associated 2DEG densities of 2.6*10/sup 12/ cm/sup -2/ were obtained at room temperature. Effects of vicinal substrates on mobilities was determined with conduction paths parallel and perpendicular to steps seen in AFM images. Finally, RF results are presented on devices with 0.25 mu m*100 mu m gate geometry.
Subfile: B

43/3,AB/5
DIALOG(R)File 2:INSPEC

5963011 INSPEC Abstract Number: A9816-7340L-010, B9808-2530B-022
Title: Interface quality and electron transfer at the GaInP on **GaAs heterojunction**
Author(s): Schuler, O.; Dehaese, O.; Wallart, X.; Mollot, F.
Author Affiliation: Inst. d'Electron et de Microelectron. du Nord, CNRS, Villeneuve, France
Journal: Journal of Applied Physics vol.84, no.2 p.765-9
Publisher: AIP,
Publication Date: 15 July 1998 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
SICI: 0021-8979(19980715)84:2L.765:IQET;1-7

Material Identity Number: J004-98013
U.S. Copyright Clearance Center Code: 0021-8979/98/84(2)/765(5)/$15.00
Language: English

Abstract: Hall measurements performed on Ga/sub 0.50/In/sub 0.50/P/In/sub 0.20/Ga/sub 0.80/As structures show abnormally low mobility both at room temperature and at 77 K, and too high electron densities which cannot be attributed to a normal two-dimensional electron gas in the channel. On the other hand, low temperature photoluminescence on asymmetrical AlGaAs/ **GaAs** /GaInP quantum wells and x-ray photoemission spectroscopy measurements reveal the presence of arsenic atoms in the GaInP barrier. Using a one-dimensional Schrodinger-Poisson simulation with a nonabrupt interface model, we show that the presence of arsenic in GaInP leads to the formation of a parasitic GaInAsP well between the delta -doped **layer** and the **channel**, trapping the main part of transferred electrons. We experimentally show that the electron transfer can be drastically improved by inserting a thin AlInP layer at the interface. Insertion of at least six monolayers of AlInP is needed to recover a normal electron transfer as high as 2.1*10/sup 12/ cm/sup -2/.

Subfile: A B

43/3,AB/6
DIALOG(R)File 2:INSPEC

5835265 INSPEC Abstract Number: A9806-6855-099, B9803-0510D-213
Title: Growth of GaInP/AlGaAs/**GaAs** structures for high power laser diodes

Author(s): Bugge, F.; Sebastian, J.; Knauer, A.; Beister, G.; Rechenberg, I.; Vogel, K.; Erbert, G.; Weyers, M.
Author Affiliation: Ferdinand-Braun Inst. fur Hochstfrequenztechnik, Berlin, Germany

Conference Title: Workshop Booklet. EW MOVPE VII. 7th European Workshop on Metal-Organic Vapour Phase Epitaxy and Related Growth Techniques p. H10 4 pp.
Publisher: Tech. Univ. Berlin, Berlin, Germany
Publication Date: 1997 Country of Publication: Germany 440 pp.
Material Identity Number: XX97-01706
Conference Title: Proceedings of European Workshop on Metal Organic Vapor Phase Epitaxy
Conference Date: 8-11 June 1997 Conference Location: Berlin, Germany

Language: English

Abstract: Results on MOVPE growth of GaInP-AlGaAs-**GaAs** laser diodes with different structures are presented. In carry-over and As/P exchange effects can occur at the AlGaAs-GaInP heterointerfaces which result in the formation of dislocations and/or parasitic quantum wells and Zn accumulation at the interfaces of p-doped layers. The use of different growth temperatures and the optimization of the growth conditions at the heterointerface strongly reduce such effects and improve the performance of the laser diodes. Broad area laser diodes grown under optimized conditions show results which are comparable to AlGaAs laser diodes. Also degradation rates of ridge waveguide laser diodes are comparable despite the lower efficiency of the AIGaAs-GaInP diodes under test. In buried structures GaInP can act as an etch stop layer and, contrary to AlGaAs, there are no problems caused by the formation of oxides. Real index self-aligned structure (RISAS) laser diodes with GaInP as waveguide and current **blocking layer** were fabricated showing output powers up to 450 mW per facet for a 5 mu m wide trench.

Subfile: A B

43/3,AB/7
DIALOG(R)File 2:INSPEC

5676083 INSPEC Abstract Number: B9710-0510D-082
Title: Hydrogen in carbon-doped **GaAs** base layer of GaInP/**GaAs** **heterojunction** bipolar transistors
Author(s): Richter, E.; Kurpas, P.; Sato, M.; Trapp, M.; Zeimer, U.; Haehle, S.; Weyers, M.
Author Affiliation: Ferdinand-Braun-Inst. fur Hochstfrequenztech., Berlin, Germany
Journal: Materials Science & Engineering B (Solid-State Materials for Advanced Technology) Conference Title: Mater. Sci. Eng. B, Solid-State Mater. Adv. Technol. (Switzerland) vol.44, no.1-3 p.337-40
Publisher: Elsevier,
Publication Date: Feb. 1997 Country of Publication: Switzerland
CODEN: MSBTEK ISSN: 0921-5107
SICI: 0921-5107(199702)44:1/3L.337:HCDG;1-Z
Material Identity Number: M712-97007
U.S. Copyright Clearance Center Code: 0921-5107/97/$17.00
Conference Title: 3rd International Workshop on Expert Evaluation and Control of Compound Semiconductor Materials and Technologies
Conference Sponsor: Deutsche Forschungsgemeinschaft; Fraunhofer IAF; Freiberger Compound Mater.; et al
Conference Date: 12-15 May 1996 Conference Location: Freiburg, Germany
Language: English
Abstract: Hydrogen incorporation into heavily carbon-doped **GaAs** grown by metal-organic vapour phase epitaxy using carbon tetrabromide (CBr/sub 4/) has been studied. In the base layer of as-grown GaInP/ **GaAs** **heterojunction** bipolar transistors (**HBTs**), about 20% of the carbon acceptors are found to be passivated by hydrogen. The outdiffusion of this hydrogen during an ex situ annealing at 450 degrees C in nitrogen, which is effective for carbon-doped single **layers**, is **blocked** by n-type capping layers in **HBTs**. An in situ annealing step was found to be suitable to reduce the acceptor passivation in **HBTs** to about 10%.
Subfile: B

43/3,AB/8
DIALOG(R)File 2:INSPEC

5555416 INSPEC Abstract Number: B9705-2560J-026
Title: MOVPE growth of GaInP/**GaAs** hetero-bipolar-transistors using CBr/sub 4/ as carbon dopant source
Author(s): Kurpas, P.; Richter, E.; Sato, M.; Brunner, F.; Gutsche, D.; Weyers, M.
Author Affiliation: Ferdinand-Braun-Inst. fur Hochstfrequenztech., Berlin, Germany
Journal: Journal of Crystal Growth Conference Title: J. Cryst. Growth (Netherlands) vol.170, no.1-4 p.442-6
Publisher: Elsevier,
Publication Date: Jan. 1997 Country of Publication: Netherlands

CODEN: JCRGAE ISSN: 0022-0248
SICI: 0022-0248(199701)170:1/4L.442:MGGG;1-6
Material Identity Number: J037-97005
U.S. Copyright Clearance Center Code: 0022-0248/97/$17.00
Conference Title: 8th International Conference on Metalorganic Vapour Phase Epitaxy
Conference Date: 9-13 June 1996 Conference Location: Cardiff, UK
Language: English

Abstract: Carbon doping of **GaAs** with carbon tetrabromide (CBr/sub 4/) in low pressure MOVPE has been investigated and applied to the fabrication of GaInP/**GaAs** **HBTs** . Especially the hydrogen incorporation and the associated acceptor passivation has been studied. The hydrogen found in single **GaAs**:C layers is predominantly incorporated during cooling the sample under AsH/sub 3/ after growth. n-type capping **layers** can **block** this H indiffusion and **GaAs**:C base layers in **HBTs** show much lower H concentrations than **GaAs**:C single layers without a cap. A further reduction of acceptor passivation is possible by optimization of the growth procedure. First **HBTs** processed from layers with a base that was doped using CBr/sub 4/ show promising DC and HF performance (beta =45, f/sub T/=26 GHz for 2*20 mu m/sup 2/ devices).

Subfile: B

43/3,AB/9
DIALOG(R)File 2:INSPEC

03789395 INSPEC Abstract Number: B91002946
Title: Advanced integrated planar InP/**InGaAs** /InP:Fe PIN-FET photoreceiver with inhomogeneous doped layer structure

Author(s): Albrecht, H.; Penz, R.; Lauterbach, C.; Hoffmann, L.; Ebbinghaus, G.; Scherg, T.; Strzoda, R.
Author Affiliation: Siemens Res. Labs., Munchen, West Germany

Conference Title: EFOC/LAN 90. The Eighth European Fibre Optic Communication and Local Area Networks Exposition. EFOC Proceedings p. 172-7
Publisher: IGI Europe, Basel, Switzerland
Publication Date: 1990 Country of Publication: Switzerland xxi+422 pp.
Conference Date: 27-29 June 1990 Conference Location: Munich, West Germany
Language: English

Abstract: An advanced integrated planar structure for a photodiode **heterojunction** field-effect transistor combination (pin-HJFET) with an inhomogeneous doped layer sequence onto a flat surface substrate is described. The optimization for the HJFET has been obtained with a local buried p-n junction beneath the **channel layer** of the HJFET. The pin-HJFET technology is outlined and the obtained device performance is discussed.

Subfile: B

43/3,AB/10
DIALOG(R)File 2:INSPEC

03708230 INSPEC Abstract Number: B90061634

Title: Ion implanted **confinement layer** for an InP/**InGaAs** /InP:Fe **heterojunction** field-effect transistor
Author(s): Lauterbach, Ch.; Romer, D.; Treichler, R.
Author Affiliation: Siemens AG, Res. Labs., Munich, West Germany
Journal: Applied Physics Letters vol.57, no.5 p.481-3
Publication Date: 30 July 1990 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
U.S. Copyright Clearance Center Code: 0003-6951/90/310481-03$02.00
Language: English
Abstract: A p-doped **confinement layer** was fabricated by Be implantation for an InP/**InGaAs**/InP:Fe **heterojunction** field-effect transistor (HFET). The epitaxial layers were grown by metalorganic vapor phase epitaxy and were suitable for the integration with a pin photodiode. The pn junction of the gate was formed by Zn diffusion that is not influenced by the preceding ion implantation. In the output characteristics of the HFET the pinch-off voltage changes from V/sub p/=-7 V without to V/sub p/=-3.5 V with **confinement layer**. No degradation of the maximum transconductance was observed. The gate leakage current is 80 nA at a gate source voltage of V/sub gs/=-5 V.
Subfile: B

43/3,AB/11
DIALOG(R)File 2:INSPEC

01951841 INSPEC Abstract Number: A82102821, B82059904
Title: Characterization of liquid phase epitaxial quaternary lasers by EBIC mode scanning electron microscopy
Author(s): Levin, E.R.; Ladany, I.
Author Affiliation: RCA Labs., David Sarnoff Res. Center, Princeton, NJ, USA
Journal: Thin Solid Films vol.90, no.4 p.372
Publication Date: 30 April 1982 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
Conference Title: Fifth International Thin Films Congress
Conference Date: 21-25 Sept. 1981 Conference Location: Herzlia on Sea, Israel
Language: English
Abstract: Summary form only given. Zero-bias EBIC line profiles obtained in conjunction with high magnification emissive mode SEM imaging were used to determine the precise location of the principal p-n junction in a **In-Ga-As-P** laser structure, identified as the position of the EBIC current maximum, relative to the physical boundaries of the LPE layers. The authors observed differences in the junction locations dependent on the type of p dopant used. In lasers incorporating cadmium doping, the p-n junction is usually observed to be in the p-InP layer, sometimes at a considerable distance (up to 0.4 mu m) from the **edge** of the cavity **layer** . Correlation of these data with measured device parameters indicates that the lasing threshold increases a with increasing distance of the junction from the cavity. In zinc-doped devices, however, the p-n junction usually appears within the cavity region, close to the boundary with the p layer. No clear relation between the junction position and the lasing threshold was observed for the case of zinc doping.
Subfile: A B

? T S56/3,AB/1-15

56/3,AB/1
DIALOG(R)File 2:INSPEC

7176388 INSPEC Abstract Number: B2002-03-1350F-023
Title: High-speed performance of NpN InGaAsN-based double **heterojunction** bipolar transistors
Author(s): Baca, A.G.; Monier, C.; Chang, P.C.; Li, N.Y.; Newman, F.; Armour, E.; Sun, S.Z.; Hou, H.Q.
Author Affiliation: Sandia Nat. Labs., Albuquerque, NM, USA
Conference Title: GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. 23rd Annual Technical Digest 2001 (Cat. No.01CH37191) p.192-5
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA ix+279 pp.
ISBN: 0 7803 6663 8 Material Identity Number: XX-2001-02425
U.S. Copyright Clearance Center Code: 0-7803-6663-8/01/$10.00
Conference Title: GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. 23rd Annual Technical Digest 2001
Conference Sponsor: IEEE Electron Devices Soc.; IEEE Microwave Theory & Tech. Soc.; IEEE Solid-State Circuits Soc
Conference Date: 21-24 Oct. 2001 Conference Location: Baltimore, MD, USA
Language: English
Abstract: We report the fabrication of double **heterojunction** bipolar transistors (DHBTs) with the use of a new quaternary InGaAsN material system that takes advantage of a low energy **band gap** in the base to reduce operating voltages in **GaAs**-based electronic devices. InGaP/In/sub 0.03/Ga/sub 0.97/As/sub 0.99/N/sub 0.01//**GaAs** DHBTs with improved **band gap** engineering at both **heterojunctions** exhibit a DC peak current gain over 16 with small active emitter area. The use of the InGaAsN base layer allows a significant reduction of the turn-on voltage by 250 mV for the new technology over a standard InGaP/**GaAs** **HBT** , while maintaining high-frequency characteristics with cut-off frequency and maximum oscillation frequency as high as 40 GHz and 70 GHz, respectively. This technology is promising for next generation RF circuits using **GaAs**-based **HBTs** by reducing the operating voltage for low power consumption and better handling of supply voltages in advanced wireless handsets.
Subfile: B

56/3,AB/2
DIALOG(R)File 2:INSPEC

7102800 INSPEC Abstract Number: B2002-01-2560J-034
Title: Polarized-photoreflectance characterization of an InGaP/InGaAsN/**GaAs** NpN double-**heterojunction** bipolar transistor structure
Author(s): Lin, C.J.; Huang, Y.S.; Li, N.Y.; Li, P.W.; Tiong, K.K.
Author Affiliation: Dept. of Electron. Eng., Nat. Taiwan Univ., Taipei, Taiwan
Journal: Journal of Applied Physics vol.90, no.9 p.4565-9
Publisher: AIP,
Publication Date: 1 Nov. 2001 Country of Publication: USA

CODEN: JAPIAU ISSN: 0021-8979
SICI: 0021-8979(20011101)90:9L.4565:PPCI;1-B
Material Identity Number: J004-2001-021
U.S. Copyright Clearance Center Code: 0021-8979/2001/90(9)/4565(5)/$18.00
Language: English

Abstract: We have characterized an InGaP/InGaAsN/**GaAs** NpN double-**heterojunction** bipolar transistor structure using polarized photoreflectance (PR) spectroscopy. The ordering parameter of the InGaP is deduced from the polarization {[110] and [110]} dependence of the PR signals from the emitter region. The ordering related piezoelectric field is also found to influence the electric field, as evaluated from observed Franz-Keldysh oscillations, in the InGaP emitter region. The field in the emitter region is found to be about 25 kV/cm smaller than the theoretical value that does not take into account the possible ordering induced screening effect, while the field in the collector region agrees well with the theoretical value. In addition, the InGaAsN **band gap** is also determined by analyzing the PR spectrum of the base region.

Subfile: B

56/3,AB/3
DIALOG(R)File 2:INSPEC

6701006 INSPEC Abstract Number: B2000-10-2560S-035

Title: A simulation study on the effect of channel thickness on the characteristics of Ga/sub 0.52/In/sub 0.48/P/In/sub 0.2/Ga/sub 0.8/As/Ga/sub 0.52/In/sub 0.48/P DH-pHEMT

Author(s): Yoon, S.F.; Kam, A.H.T.; Zheng, H.Q.; Gay, B.P.
Author Affiliation: Sch. of Electr. & Electron. Eng., Nanyang Technol. Univ., Singapore

Journal: Microelectronics Journal vol.31, no.8 p.667-76
Publisher: Elsevier,
Publication Date: Aug. 2000 Country of Publication: UK
CODEN: MICEB9 ISSN: 0026-2692
SICI: 0026-2692(200008)31:8L.667:SSEC;1-6
Material Identity Number: M243-2000-006
U.S. Copyright Clearance Center Code: 0026-2692/2000/$20.00
Language: English

Abstract: The dc performance of a Ga/sub 0.52/In/sub 0.48/P/In/sub 0.2/Ga/sub 0.8/As/Ga/sub 0.52/In/sub 0.48/P double **heterojunction** pseudomorphic high electron mobility transistor (DH-pHEMT) grown on **GaAs** substrate has been simulated using a two-dimensional device simulator, to investigate the dependence of the intrinsic and extrinsic transconductance on the device channel thickness. The electron sheet concentration values for different channel thicknesses have been calculated using an analytical model, and correspond very well to Hall effect measurements of the electron mobility. Simulation results reveal that the optimum channel thickness for maximum intrinsic transconductance is between 80 and 100 AA, while there is no significant difference in the maximum extrinsic transconductance for channel thicknesses between 80 and 140 AA. This is due to a tradeoff between electron sheet concentration and gate-to-channel separation. In addition, narrow channels give larger effective **band gap** due to energy quantization, which could contribute to an optimum design for Ga/sub 0.52/In/sub 0.48/P/In/sub 0.2/Ga/sub 0.8/As/Ga/sub 0.52/In/sub 0.48/P DH-pHEMTs.

Subfile: B

56/3,AB/4
DIALOG(R)File 2:INSPEC

6567516 INSPEC Abstract Number: A2000-11-7340L-001, B2000-06-2530B-001
Title: Effect of **GaAs**/sub y/P/sub 1-y/(0<or=y<1) interlayers on the structural, optical, and electrical characteristics of **GaAs**/InGaP **heterojunction**
Author(s): Yong-Hwan Kwon; Jeong, W.G.; Yong-Hoon Cho; Byung-Doo Choe
Author Affiliation: Dept. of Phys., Seoul Nat. Univ., South Korea
Journal: Applied Physics Letters vol.76, no.17 p.2379-81
Publisher: AIP,
Publication Date: 24 April 2000 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(20000424)76:17L.2379:EGIS;1-F
Material Identity Number: A135-2000-017
U.S. Copyright Clearance Center Code: 0003-6951/2000/76(17)/2379(3)/$17.0
0
Language: English
Abstract: The effect of **GaAs**/sub y/P/sub 1-y/(0<or=y<1) interlayers on the characteristics of **GaAs**/InGaP **heterojunction** has been investigated. For samples having **GaAs**/sub y/P/sub 1-y/ interlayers in the range of 0<y<or=0.75 inserted in the **GaAs**-on-InGaP interface, sharp **GaAs** band-edge emissions are recovered. These results are attributed to smoothly grown **InGaAs**(P) interfacial layers with the **band-gap** energy higher than that of **GaAs** through transmission electron microscopy measurements. In addition, the amount of carrier depletion at the **GaAs**-on-InGaP interface is smaller with the use of **GaAs**/sub y/P/sub 1-y/ interlayers than that for no interlayer in capacitance-voltage measurements.
Subfile: A B

56/3,AB/5
DIALOG(R)File 2:INSPEC

6559915 INSPEC Abstract Number: B2000-05-2560J-023
Title: InGaP/InGaAsN/**GaAs** NpN double-**heterojunction** bipolar transistor
Author(s): Chang, P.C.; Baca, A.G.; Li, N.Y.; Xie, X.M.; Hou, H.Q.; Armour, E.
Author Affiliation: Sandia Nat. Labs., Albuquerque, NM, USA
Journal: Applied Physics Letters vol.76, no.16 p.2262-4
Publisher: AIP,
Publication Date: 17 April 2000 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(20000417)76:16L.2262:IIGD;1-5
Material Identity Number: A135-2000-016
U.S. Copyright Clearance Center Code: 0003-6951/2000/76(16)/2262(3)/$17.0
0
Language: English
Abstract: We have demonstrated a functional NpN double-**heterojunction** bipolar transistor (DHBT) using InGaAsN for the base layer. The InGaP/In/sub 0.03/Ga/sub 0.97/As/sub 0.99/N/sub 0.01//**GaAs** DHBT has a low V/sub ON/ of 0.81 V, which is 0.13 V lower than in a InGaP/

GaAs heterojunction bipolar transistor (**HBT**). The lower turn-on voltage is attributed to the smaller **band gap** (1.20 eV) of metalorganic chemical vapor deposition-grown In/sub 0.03/Ga/sub 0.97/As/sub 0.99/N/sub 0.01/ base layer. **GaAs** is used for the collector; thus the breakdown voltage (BV/sub CEO/) is 10 V, consistent with the BV/sub CEO/ of InGaP/**GaAs HBTs** of comparable collector thickness and doping level. To alleviate the current blocking phenomenon caused by the larger conduction band discontinuity between InGaAsN and **GaAs**, a graded **InGaAs** layer with delta doping is inserted at the base-collector junction. The improved device has a peak current gain of seven with ideal current-voltage characteristics.
Subfile: B

56/3,AB/6
DIALOG(R)File 2:INSPEC

6305882 INSPEC Abstract Number: B1999-09-1350H-003
Title: Millimeter-wave monolithic IC technology for 60-GHz application
Author(s): Watanabe, Y.; Okubo, N.
Author Affiliation: Fujitsu Labs. Ltd., Atsugi, Japan
Conference Title: 1997 International Conference on GaAs Manufacturing Technology. Digest of Papers p.54-7
Publisher: GaAs MANTECH Conference, St. Louis, MN, USA
Publication Date: 1997 Country of Publication: USA 179 pp.
Material Identity Number: XX-1997-01703
Conference Title: Proceedings of International Conference on GaAs Manufacturing. MANTECH 97
Conference Sponsor: Hughes; Texas Instruments; GEC-Marconi; Northrop Grumman; Oki Electric; M/A-COM; Emcore; Raytheon; Daimler-Benz; TLC Precision; Freiberger; Picogiga; Fujitsu; Hewlett Packard; Kopin; Motorola; Sumitomo Electric; Watkins-Johnson; QED; Airtron; GaAstronics; ITT
Conference Date: 2-5 June 1997 Conference Location: San Francisco, CA, USA
Language: English
Abstract: We have developed a **heterojunction** device technology for use in high frequency communication systems, based on epitaxial growth on a **GaAs** substrate. Both our high electron mobility transistor (HEMT) and **heterojunction** bipolar transistor (**HBT**) use InGaP as a wide bandgap layer in their device structures and exhibit high frequency performance with high reliability. A millimeter-wave automotive radar system has been fabricated with the 60 GHz monolithic HEMT ICs using wafer thinning and the plated heat sink technique.
Subfile: B

56/3,AB/7
DIALOG(R)File 2:INSPEC

5978395 INSPEC Abstract Number: B9809-2560J-003
Title: GaInP-AlGaAs-GaInP double **heterojunction** bipolar transistors with zero conduction band spike at the collector
Author(s): Lye, B.C.; Yow, H.K.; Houston, P.A.; Button, C.C.
Author Affiliation: Dept. of Electron. & Electr. Eng., Sheffield Univ., UK

Conference Title: WOCSDICE 97. 21st Workshop on Compound Semiconductor Devices and Integrated Circuits p.124-5
Editor(s): van der Roer, T.G.
Publisher: Eindhoven Univ. Technol, Eindhoven, Netherlands
Publication Date: 1997 Country of Publication: Netherlands 142 pp.
ISBN: 90 9010 767 3 Material Identity Number: XX97-01702
Conference Title: Proceedings of WOCSDICE 97. 21st Workshop on Compound Semiconductor Devices and Integrated Circuits
Conference Date: 25-28 May 1997 Conference Location: Scheveningen, Netherlands
Language: English
Abstract: Summary form only given. GaInP-**GaAs**-GaInP double **heterojunction** bipolar transistors (DHBTs) make use of the large breakdown voltage offered by the wide gap collector for high power applications. However, the conduction band spike at the abrupt **GaAs** -GaInP base-collector junction gives rise to an undesirable voltage dependence of gain at low collector-emitter bias. Solutions to this problem include the incorporation of an undoped **GaAs** spacer layer, adjacent to the GaInP collector, and/or an n/sup +/ doping region in the vicinity of the spike to encourage tunnelling. Drawbacks to these methods are the reduced Kirk effect current and tunnelling breakdown if the n/sup +/ layer is not positioned accurately. We present a novel approach to eliminate the conduction band spike using AlGaAs as the base material, which has been shown to have a zero conduction band offset with GaInP for an Al concentration in the group III sublattice of >or=11%.
Subfile: B

56/3,AB/8
DIALOG(R)File 2:INSPEC

5956232 INSPEC Abstract Number: A9815-8115H-060, B9808-0510D-086
Title: Fabrication and I-V-T behaviour of n-**GaAs**/semi-insulating GaInP:Fe/n-**GaAs** structures
Author(s): Lourdudoss, S.; Holz, R.
Author Affiliation: Dept. of Electron., R. Inst. of Technol., Kista, USA
Journal: Journal of Crystal Growth vol.179, no.3-4 p.371-81
Publisher: Elsevier,
Publication Date: Aug. 1997 Country of Publication: Netherlands
CODEN: JCRGAE ISSN: 0022-0248
SICI: 0022-0248(199708)179:3/4L.371:FBGS;1-5
Material Identity Number: J037-97019
U.S. Copyright Clearance Center Code: 0022-0248/97/$17.00
Language: English
Abstract: The n-**GaAs**:S/SI-GaInP:Fe/n-**GaAs** (substrate) structures with various Fe concentrations in the SI (semi-insulating) GaInP:Fe layer have been fabricated by hydride vapour-phase epitaxy and their I-V curves studied at temperatures up to 473 K. Certain amount of diffusion of Fe into the **GaAs** substrate and accumulation of Fe at the interface are related to the nature of the incorporated Fe. The I-V behaviour is different depending upon the Fe concentration. The conductivity derived from the I-V curves exhibits a minimum at a certain concentration of Fe at which the compensation is maximum. It is suggested that Fe is mostly site-incorporated and interstitially located in the low concentration regime and mostly in the form of FeP precipitates in the high concentration regime and a mixture of two in the intermediate regime. At low voltages, the activation energy calculated from the current density

versus 1/T curves yields the Fe level in the **band gap** corresponding to the value previously cited in the literature. Frenkel-Poole effect is found to be operative at certain high field regions. Conductivity at T to infinity for various Fe concentrations has been derived and found to follow the same trend as that has been observed at the experimental temperatures. The extent of compensation in the considered samples also gets reflected in the slope of the I-V curve in the trap-filled-regime.
Subfile: A B

56/3,AB/9
DIALOG(R)File 2:INSPEC

5074446 INSPEC Abstract Number: A9522-7320-001, B9511-2530B-036
Title: Determination of Al mole fraction for null conduction band offset in In/sub 0.5/Ga/sub 0.5/P/Al/sub x/Ga/sub 1-x/As **heterojunction** by photoluminescence measurement
Author(s): Kwan-Shik Kim; Yong-Hoon Cho; Byung-Doo Choe; Weon Guk Jeong; Lim, H.
Author Affiliation: Dept. of Phys., Seoul Nat. Univ., South Korea
Journal: Applied Physics Letters vol.67, no.12 p.1718-20
Publication Date: 18 Sept. 1995 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
U.S. Copyright Clearance Center Code: 0003-6951/95/67(12)/1718/3/$6.00
Language: English
Abstract: Photoluminescence properties of In/sub 0.5/G/sub 0.5/P/Al/sub x/Ga/sub 1-x/As **heterojunctions** in both staggered and straddling band alignment regimes have been investigated. From the relation between the energies of below-**band gap** luminescence and Al compositions in the staggered band alignment regime, we determined the Al composition for null conduction band offset of the **heterojunction** as well as the conduction band offset value of In/sub 0.5/Ga/sub 0.5/P/**GaAs heterojunction**. Assuming the transitivity between the conduction band offset valves, we also obtained the fraction of the **band gap** energy difference that is associated with the conduction band offset of an AlGaAs/**GaAs heterojunction**.
Subfile: A B

56/3,AB/10
DIALOG(R)File 2:INSPEC

4963697 INSPEC Abstract Number: A9513-8115G-008, B9507-0510D-057
Title: Solid source molecular-beam epitaxial growth of Ga/sub 0.5/In/sub 0.5/P using a valved, three-zone phosphorus source
Author(s): Hoke, W.E.; Weir, D.G.; Lemonias, P.J.; Hendriks, H.T.; Jackson, G.S.; Colombo, P.
Author Affiliation: Res. Div., Raytheon Co., Lexington, MA, USA
Journal: Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures) vol.13, no.2 p.733-5
Publication Date: March-April 1995 Country of Publication: USA
CODEN: JVTBD9 ISSN: 0734-211X
U.S. Copyright Clearance Center Code: 0734-211X/95/13(2)/733/3/$6.00
Conference Title: 14th North American Conference on Molecular-Beam

Epitaxy
Conference Date: 10-12 Oct. 1994 Conference Location: Urbana, IL, USA
Language: English
Abstract: Ga/sub 0.5/In/sub 0.5/P/**GaAs heterojunction** films were grown using a valved, three-zone phosphorus source and valved arsenic source. The design of the phosphorus source eliminates the flux bursts experienced upon valve opening with two-zone furnaces. Narrow x-ray linewidths with Pendellosung interference oscillations were observed in double crystal measurements. Chemically abrupt As/P and P/As interfaces were obtained using both valved sources. The optical **band gap** determined from photoluminescence was consistent with minimal ordering in the films. GaInP films were doped with silicon in the 10/sup 17/ cm/sup -3/ range with good mobilities and negligible carrier freeze-out upon cooling. A GaInP(emitter)/**GaAs** (5*10/sup 19/ cm/sup -3/ carbon doped base) **heterojunction** bipolar transistor exhibited a current gain of 30.
Subfile: A B

56/3,AB/11
DIALOG(R)File 2:INSPEC

4863805 INSPEC Abstract Number: A9504-6825-009, B9503-0510D-018
Title: Strain relaxation of Ga/sub 0.2/In/sub 0.8/As and InAs/sub 0.5/P/sub 0.5/ layers grown on InP substrate for 1.6 to 2.4 mu m spectral range Ga/sub x/In/sub 1-x/As/InAs/sub y/P/sub 1-y//InP photodiodes application
Author(s): Kae-Nune, P.; di Forte-Poisson, M.A.; Brylinski, C.; di Persio, J.
Author Affiliation: Thomson-CSF, Orsay, France
p.135
Publisher: IEEE, New York, NY, USA
Publication Date: May 1993 Country of Publication: USA xx+738 pp.
ISBN: 0 7803 0993 6
Conference Title: 1993 (5th) International Conference on Indium Phosphide and Related Materials
Conference Sponsor: IEEE; Societe des Electriciens et des Electroniciens
Conference Date: 19-22 April 1993 Conference Location: Paris, France
Language: English
Abstract: Mismatched Ga/sub 1-x/As/InAs/sub y/P/sub 1-y//InP double heterostructures were prepared by the low pressure-metal-organic chemical vapor deposition (LP-MOCVD) epitaxial technique for optical photodiode application in the 1.6 mu m-2.4 mu m range. The required narrow **band gap** active layer consists of a high indium composition Ga/sub 1-x/In/sub x/As (x = 0.8) layer. Different graded composition and superlattice buffer layers are investigated to accommodate the 1.8% lattice mismatch between InP and Ga/sub 0.2/In/sub 0.8/As. It is shown that a two microns thick InAs/sub y/P/sub 1-y/ graded composition layer (y up to 0.5) presents better optical and structural properties than a Ga/sub 1-x/In/sub x/As graded composition layer. High resolution X-ray diffraction investigations of an InAs/sub y/P/sub 1-y//Ga/sub 1-x/I superlattice shows its good ability to act as a barrier to dislocation propagation.
Subfile: A B

56/3,AB/12
DIALOG(R)File 2:INSPEC

4520971 INSPEC Abstract Number: A9324-8630J-011, B9312-2560H-028
Title: AlGaAs/GaInP **heterojunction** tunnel diode for cascade solar cell application
Author(s): Jung, D.; Parker, C.A.; Ramdani, J.; Bedair, S.M.
Author Affiliation: Dept. of Electr. & Comput. Eng., North Carolina State Univ., Raleigh, NC, USA
Journal: Journal of Applied Physics vol.74, no.3 p.2090-3
Publication Date: 1 Aug. 1993 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
U.S. Copyright Clearance Center Code: 0021-8979/93/74(3)/2090/4/$6.00
Language: English
Abstract: A p/sup +/-AlGaAs/n/sup +/-GaInP **heterojunction** tunnel diode with **band gap** E/sub g/ approximately=1.9 eV was fabricated by the atomic layer epitaxy growth. Doping levels of 1*10/sup 20/ cm/sup -3/ and 5*10/sup 19/ cm/sup -3/ were achieved in the p and n side of the diode using carbon and selenium, respectively. The diode can be used to interconnect the high and low **band-gap** cells in the AlGaAs/**GaAs** cascade solar cell structure. For forward current of 20 A/cm/sup 2/, which is the expected current density at 1000 suns operation, there is only approximately 20 mV voltage drop across the tunnel junction. When annealed at 650 and 750 degrees C to simulate the growth of the top cell, the diode was still suitable for 1000 suns operation. This is the first reported tunnel diode fabricated in high **band-gap** material systems that can be used as the connecting junction in the cascade solar cell structure operating at 1000 suns.
Subfile: A B

56/3,AB/13
DIALOG(R)File 2:INSPEC

4446739 INSPEC Abstract Number: A9317-7340L-006, B9309-2560H-001
Title: AlGaAs/GaInP **heterojunction** tunnel diode
Author(s): Jung, D.; Parker, C.A.; Ramdani, J.; Bedair, S.M.
Author Affiliation: Dept. of Electr. & Comput. Eng., North Carolina State Univ., Raleigh, NC, USA
Journal: AIP Conference Proceedings no.268 p.338-43
Publication Date: 1992 Country of Publication: USA
CODEN: APCPCS ISSN: 0094-243X
U.S. Copyright Clearance Center Code: 0094-243X/92/$2.00
Conference Title: Photovoltaic Advanced Research and Development Project
Conference Date: 1992 Conference Location: Denver, CO, USA
Language: English
Abstract: A p/sup +/-AlGaAs/n/sup +/-GaInP **heterojunction** tunnel diode with **band gap** E/sub g/ approximately=1.9 eV was fabricated by atomic layer epitaxy growth mode using carbon and selenium as the p- and n-type dopants, respectively. The doping levels of 1*10/sup 20//cm/sup 3 /and 5*10/sup 19//cm/sup 3/ were achieved both in the p- and n-side of the diode, respectively. The diode can be used as the interconnection of the high and low **band gap** cells in the AlGaAs/**GaAs** cascade solar cell structure. At the forward current of 15 A/cm/sup 2/, which is the expected current density at 1000 suns operation, there is only approximately 17 mV voltage drop across the tunnel junction. This is the first reported tunnel diode fabricated in high **band gap** material systems, with performances that exceed the best reported **GaAs** tunnel diode.

03/11/2002 Serial No.:09/893,477

Subfile: A B

56/3,AB/14
DIALOG(R)File 2:INSPEC

04260635 INSPEC Abstract Number: B9212-2560J-002
Title: Improved performance of carbon-doped **GaAs** base **heterojunction** bipolar transistors through the use of InGaP
Author(s): Abernathy, C.R.; Ren, F.; Wisk, P.W.; Pearton, S.J.; Esagui, R.
Author Affiliation: AT&T Bell Labs., Murray Hill, NJ, USA
Journal: Applied Physics Letters vol.61, no.9 p.1092-4
Publication Date: 31 Aug. 1992 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
U.S. Copyright Clearance Center Code: 0003-6951/92/341092-03$03.00
Language: English
Abstract: Carbon-doped **GaAs**/AlGaAs **heterojunction** bipolar transistors (**HBTs**) typically exhibit severe leakage at the base-emitter interface which limits their utility for low-current applications. Furthermore, the device breakdown voltage, and hence power handling capability, is limited due to the **band gap** of the **GaAs** collector material. In this letter the authors will demonstrate for the first time that both of these limitations can be overcome through the use of InGaP. Since InGaP is not readily doped with carbon, it does not suffer from compensation due to carryover of carbon from the **GaAs** base. Hence, the ideality factor of the base-emitter junction improves from 1.3 to 1.09 when the conventional n-AlGaAs emitter layer is replaced with n-InGaP. Moreover, InGaP eliminates the crossover of the base and collector currents typically observed in heavily carbon doped **GaAs HBTs**. This results in the maintenance of gain even at very low collector currents. As a collector material, they have found that InGaP produces significantly higher breakdown voltage than **GaAs** (19 V vs. 12 V) of the same thickness and doping, due to its larger **band gap**. As in the emitter, InGaP collectors exhibit excellent ideality factors of approximately 1.05.
Subfile: B

56/3,AB/15
DIALOG(R)File 2:INSPEC

03847439 INSPEC Abstract Number: A91049003
Title: Optical investigation of the band offsets in an **InGaAs** -InGaAsP-InP double-step quantum well
Author(s): Soucail, B.; Voisin, P.; Voos, M.; Rondi, D.; Nagle, J.; de Cremoux, B.
Author Affiliation: Lab. de Phys. de la Matiere Condensee, Ecole Normale Superieure, Paris, France
Journal: Superlattices and Microstructures vol.8, no.3 p.279-82
Publication Date: 1990 Country of Publication: UK
CODEN: SUMIEK ISSN: 0749-6036
U.S. Copyright Clearance Center Code: 0749-6036/90/070279+04$02.00/0
Language: English
Abstract: The authors report optical investigations of an **InGaAs** -InGaAsP-InP double-step quantum well designed to provide a sensitive measurement of the band offsets in this technologically important system.

The results yield a conduction band offset to **band gap** difference ratio of 43+or-2%. This value coincides with recent determinations of this parameter in the InP-**InGaAs** **heterojunction**.
Subfile: A

```
     FILE 'REGISTRY' ENTERED AT 12:05:37 ON 11 MAR 2002
L1          156 S (GA AND AS)/ELS AND 2/ELC.SUB
L2          129 S (GA AND AS AND SB)/ELS AND 3/ELC.SUB
L3          126 S (IN AND GA AND SB)/ELS AND 3/ELC.SUB
L4          115 S (IN AND P)/ELS AND 2/ELC.SUB
L5           48 S (IN AND P AND SB)/ELS AND 3/ELC.SUB
L6          155 S (IN AND AS AND SB)/ELS AND 3/ELC.SUB
L7            1 S INDIUM/CN
                E ANTIMONY/CN
L8            1 S E3
L9            1 S GALLIUM/CN
                E PHOSPHOROUS/CN

     FILE 'HCAPLUS' ENTERED AT 12:11:56 ON 11 MAR 2002
L10      150835 S GAAS OR GALLIUM()MONOARSENIDE OR GALLIUM()ARSENIDE OR L1
L11         494 S GAASSB OR L2
L12         641 S INGASB OR L3
L13      151570 S INDIUM OR IN OR L7
L14      135999 S ANTIMONY OR SB OR L8
L15       42185 S INP OR INDIUM()PHOSPHIDE OR INDIUM()MONOPHOSPHIDE OR L4
L16          68 S INPSB OR L5
L17         564 S INASSB OR L6
L18     1465930 S GALLIUM OR GA OR L9
L19     1963976 S PHOSPHOROUS OR P
L20       31750 S HBT OR HBTS OR HETERO()JUNCTION? OR HETEROJUNCTION?
L21        3064 S SCHOTTKY(2N)CONTACT
L22       31339 S (TRENCH## OR HOLE# OR GROOVE# OR CHANNEL OR EDGE# OR FLUSH OR
L23       37824 S (BARRIER OR BLOCK? OR CONFIN?)(2N)(LAYER? OR FILM OR FILMS OR
L24         176 S (GRADED)(2N)(CHANNEL OR TRENCH## OR HOLE# OR GROOVE# OR CHANN
L25       35479 S BAND GAP
L26        1458 S SOURCE ()ELECTRODE
L27        2843 S DRAIN()ELECTRODE
L28       15501 S L20 AND L10

     FILE 'REGISTRY' ENTERED AT 12:19:19 ON 11 MAR 2002
L29         362 S (IN AND AS AND GA)/ELS AND 3/ELC.SUB

     FILE 'HCAPLUS' ENTERED AT 12:19:47 ON 11 MAR 2002

     FILE 'REGISTRY' ENTERED AT 12:21:00 ON 11 MAR 2002

     FILE 'HCAPLUS' ENTERED AT 12:22:27 ON 11 MAR 2002
L30        2707 S L28 AND (INGAAS OR L29)
L31          11 S L30 AND L24
L32         129 S L30 AND L22
L33           9 S L32 AND L25
L34          34 S L32 AND L23
L35           1 S L34 AND L21
L36           8 S L32 AND L21
L37           1 S L34 AND (L26 OR L27)
L38          18 S (L33 OR L35 OR L36 OR L37) NOT L31
L39          86 S L30 AND (CONTACT(2N)(LAYER? OR FILM OR COAT####))
L40           0 S L39 AND L26
L41           2 S L39 AND L27
L42          13 S L39 AND L23
L43          12 S L42 NOT (L31 OR L33 OR L35 OR L36 OR L37 OR L41)
L44           3 S L2(L)L22
L45           0 S L3(L)L22
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L46          38 S L30 AND (L11 OR L12)
L47           0 S L46 AND L24
L48           4 S L46 AND L22
L49           2 S L48 NOT (L31 OR L33 OR L35 OR L36 OR L37 OR L41 OR L42 OR L44
L50          38 S L46 AND (L13 OR L14)
L51           4 S L46 AND L23
L52          38 S L46 AND (L27 OR L28)
L53           1 S L46 AND GATE ELECTRODE
L54           2 S L46 AND SCHOTTKY
L55           1 S L54 NOT (L31 OR L33 OR L35 OR L36 OR L37 OR L41 OR L42 OR L44
L56        1017 S L30 AND L15

     FILE 'REGISTRY' ENTERED AT 13:00:38 ON 11 MAR 2002
L57         123 S (IN AND AS AND P)/ELS AND 3/ELC.SUB

     FILE 'HCAPLUS' ENTERED AT 13:01:51 ON 11 MAR 2002
L58         733 S L57 OR INASP
L59          35 S L56 AND (L58 OR L11 OR L16)
L60          34 S L59 AND (L13 OR L14)
L61           4 S L60 AND L22
L62           1 S L61 NOT (L31 OR L33 OR L35 OR L36 OR L37 OR L41 OR L42 OR L44
L63           2 S L60 AND L23
L64           0 S L61 NOT (L31 OR L33 OR L35 OR L36 OR L37 OR L41 OR L42 OR L44
L65           0 S L60 AND L24
L66           4 S L60 AND L25-27
L67           2 S L66 NOT (L31 OR L33 OR L35 OR L36 OR L37 OR L41 OR L42 OR L44
L68          52 S L52 OR L60
L69          41 S L68 NOT (L31 OR L33 OR L35 OR L36 OR L37 OR L41 OR L42 OR L44
```

=> D BIB AB 1-4 L31

L31 ANSWER 1 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:507766 HCAPLUS
DN 133:328032
TI Investigation of a **graded channel InGaAs/**
GaAs heterostructure transistor
AU Li, Yih-Juan; Su, Jan-Shing; Lin, Yu-Shyan; Hsu, Wei-Chou
CS Department of Electrical Engineering, National Cheng-Kung University, Tainan, Taiwan
SO Superlattices Microstruct. (2000), 28(1), 47-54
CODEN: SUMIEK; ISSN: 0749-6036
PB Academic Press
DT Journal
LA English
AB An **InGaAS/GaAs** heterostructure transistor using a **graded** InxGa1-xAs **channel** grown by low-pressure metalorg. CVD was demonstrated. A neg. differential resistance (NDR) phenomenon is obsd. Electron mobilities are significantly improved by using the **graded InGaAs channel**. For the In compn. varying from x = 0.25 (at the buffer-channel interface) to x = 0.1 (at the spacer-channel interface) structure, a peak extrinsic transconductance of 24.6 S mm - 1(at VDS = 6.5 V, VGSstep = - 0.5 mV) and a satn. c.d. .ltoreq.555 mA mm - 1for a gate length of 1.5 .mu. m were obtained. (c) 2000 Academic Press.
RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 2 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:693127 HCAPLUS
DN 131:330697
TI Improved double delta-doped (In,Ga)As/**GaAs** heterostructures with symmetric **graded channel**
AU Li, Y. J.; Shieh, H. M.; Su, J. S.; Kao, M. J.; Hsu, W. C.
CS Department of Electrical Engineering, National Cheng-Kung University, Tainan, Taiwan
SO Mater. Chem. Phys. (1999), 61(3), 266-269
CODEN: MCHPDR; ISSN: 0254-0584
PB Elsevier Science S.A.
DT Journal
LA English
AB Improved delta-doped (.delta.-doped) (In,Ga)As/**GaAs** FET transistors by grading both sides of the (In,Ga)As channel are grown by metalorg. CVD deposition. With the In compn. linearly varied from x = 0.18 at the **GaAs**/(In,Ga)As heterointerface to x = 0.25 at the center of the (In,Ga)As channel, significantly enhanced mobility due to reduced scattering is achieved when compared to that without graded heterostructure. A distinguishable two-dimensional electron gas from Shubnikov-de Hass measurements is obsd. Meanwhile, an improved extrinsic transconductance of 300 mS/mm with gate length of 1.2 .mu.m is obtained.
RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 3 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:282216 HCAPLUS
DN 129:21872
TI Characteristics of doping- and composition-**graded** doped **channel** HFET's with AlGaAs gate insulator optical gain

AU Hung, L. T.; Lour, W. S.
CS Department of Electrical Engineering, National Taiwan Ocean University, Chi-lung, Taiwan
SO Solid-State Electron. (1998), 42(3), 363-368
CODEN: SSELA5; ISSN: 0038-1101
PB Elsevier Science Ltd.
DT Journal
LA English
AB We review the recent investigation and comparison of **heterojunction** field-effect transistors (HFET's) with a variety of doped channels. The doped channels used in the studied HFET's include uniformly doped **GaAs**. **InGaAs**, compn.-graded **InGaAs/GaAs**, and doping-**graded InGaAs channels**. All of the devices have an undoped AlGaAs layer used as gate insulator. So, the parallel conduction and transconductance suppression could be avoided totally. In the case of uniformly doped-channel HFET's, an **InGaAs** channel exhibits better electron transport properties than a **GaAs** one. The corresponding extrinsic transconductance, breakdown voltage and output conductance are 130(152) mS mm-1, 17(15) V, and 2(0.3) mS mm-1 for a **GaAs** (an **InGaAs**) channel. Further improvement by using compn.- or doping-**graded channel**, electron mobility, transconductance, and breakdown voltage are enhanced. We obtained a breakdown voltage larger than 25 V and a transconductance of 184 mS mm-1 with a large gate voltage swing of 3.0 V.

L31 ANSWER 4 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:676999 HCAPLUS
DN 128:17629
TI Low-distortion AlGaAs/**InGaAs** power HFETs with quantum-doped **graded**-like **channels**
AU Lour, W. S.; Chen, H. R.; Hung, L. T.
CS Department of Electrical Engineering, National Taiwan Ocean University, Chi-lung, Taiwan
SO Semicond. Sci. Technol. (1997), 12(10), 1210-1216
CODEN: SSTEET; ISSN: 0268-1242
PB Institute of Physics Publishing
DT Journal
LA English
AB The authors report on the fabrication and characterization of quantum-doped **graded**-like **channel heterojunction** field-effect transistors (HFETs) by MBE using a multiple pulse doping technique. The extended equations describing the piecewise doping profiles were developed to derive the transconductance and 2nd-harmonic to fundamental ratio. The thickness of depletion width dominates the max. transconductance and the high doping gradient offers the device linearity. Two HFETs with different doping gradients were fabricated to elucidate this concept. The authors obtain the max. extrinsic transconductance of 165 mS mm-1. Both have broad plateaus on their transconductance vs. gate-to-source voltage profiles. Further, the devices exhibit a gate-to-drain and a drain-to-source breakdown voltage larger than 25 V. The very small output conductance and good pinch-off characteristics indicate good confinement of the electrons in a quantum-doped channel.

=> D BIB AB 5-11 L31

L31 ANSWER 5 OF 11 HCAPLUS COPYRIGHT 2002 ACS

AN 1997:296126 HCAPLUS
DN 127:58775
TI Multiple pulse-doped channel AlGaAs/**InGaAs/GaAs** HFET's
AU Lour, W. S.; Hung, L. T.; Chang, W. L.; Lia, C. Y.; Hsieh, J. L.
CS Department of Electrical Engineering, National Taiwan Ocean University, Chi-lung, Taiwan
SO Proc. - Electrochem. Soc. (1997), 97-1(Twenty-Sixth State-of-the-Art Program on Compound Semiconductors, 1997), 195-201
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
AB This paper reports on the fabrication and characterization of multiple pulse-doped channel AlGaAs/**InGaAs/GaAs** **heterojunction** field-effect transistors (HFET's). Multiple pulse-doped sheets, .delta.(n1)=1.2.times.1012, .delta.(n2)=4.times.1011, .delta.(n3)=1.times.1011 cm-2 from buffer to gate is used as an active channel. Typical drain-to-source and gate-to-drain breakdown voltages are larger than 25 V. The further enhancement in breakdown voltage is using the following methodol.: (1) a strained AlGaAs insulator, (2) **InGaAs** quantum-well like channel, (3) less impurity scattering in the **graded** pulse-doped **channel**. The max. transconductance is 160 mS/mm with an available c.d. of 250 mA/mm. Further increasing the .delta.(n1) to 4.times.1012 cm-2, the max. transconductance is 165 mS/mm. The available c.d. is increased to 480 mA/mm. Moreover, their transconductance vs. gate voltage profiles display broad plateaus. The fabricated devices exhibit a small output conductance of 0.3 mS/mm. The evaluated open-drain voltage gain is as high as 500.

L31 ANSWER 6 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:256135 HCAPLUS
DN 126:350206
TI Characterization of **graded** pulse-doped **channel** AlGaAs/**InGaAs/GaAs** **heterojunction** field-effect transistors
AU Lour, Wen-Shiung; Chen, H. R.; Hung, Ling-Tze
CS Department of Electrical Engineering, National Taiwan Ocean University, Chi-lung, Taiwan
SO Jpn. J. Appl. Phys., Part 1 (1997), 36(3A), 975-979
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB This paper reports on the fabrication and characterization of **graded** pulse-doped **channel** AlGaAs/**InGaAs/GaAs** **heterojunction** field-effect transistors (HFET's). Triple pulse-doped sheets, .delta.(n1) = 1.2 .times. 1012, .delta.(n2) = 4 .times. 1011, .delta.(n3) = 1 .times. 1011 cm-2 from buffer to gate is used as an active channel. Typical drain-to-source and gate-to-drain breakdown voltages are larger than 25 V. The further enhancement in breakdown voltage is using the following methodol.: (1) a strained AlGaAs insulator, (2) an **InGaAs** quantum-well like channel, and (3) less impurity scattering in the **graded** pulse-doped **channel**. The max. transconductance is 160 mS/mm with an available c.d. of 250 mA/mm. Further increasing the .delta.(n1) to 4 .times. 1012 cm-2, the max. transconductance is 165 mS/mm. The available c.d. is increased to 480 mA/mm. Moreover, their transconductance vs. gate voltage profiles display broad plateaus. The fabricated devices exhibit a small output conductance of 0.3 mS/mm. The evaluated open-drain voltage gain is as

high as 500. These results have better performances than those of i-AlGaAs/n+-**InGaAs** HFET's fabricated by the authors' system.

L31 ANSWER 7 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:146643 HCAPLUS
DN 126:219137
TI Controllable drain cut-in voltage with strong negative differential resistance in **GaAs**/(In,Ga)As real-space transfer heterostructure
AU Shu, Jan-Shing; Hsu, Wei-Chou; Lin, Yu-Shyan; Lin, Wei
CS Dep. Electrical Eng., National Cheng Kung Univ., Taichung, Peop. Rep. China
SO Appl. Phys. Lett. (1997), 70(8), 1002-1004
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB Three-terminal **GaAs**/(In,Ga)As/**GaAs** pseudomorphic real-space transfer heterostructure employing **graded channel** as the emitter layer grown by low-pressure metalorg. CVD deposition has been fabricated. The authors observe controllable drain cut-in voltage characteristics with strong neg. differential resistance. The largest peak-to-valley current ratio of the proposed device is about 33,000 at room temp. Moreover, the authors observe an energy exchange effect between electrons.

L31 ANSWER 8 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:752831 HCAPLUS
DN 126:151127
TI **InGaAs**-**GaAs** pseudomorphic heterostructure transistors prepared by MOVPE
AU Liu, Wen-Chau; Laih, Lih-Wen; Tsai, Jung-Hui; Lin, Kun-Wei; Cheng, Chin-Chuan
CS Department of Electrical Engineering, National Cheng-Kung University, 1 University Road, Tainan, Taiwan
SO J. Cryst. Growth (1997), 170(1-4), 438-441
CODEN: JCRGAE; ISSN: 0022-0248
PB Elsevier
DT Journal
LA English
AB The authors will demonstrate two new **InGaAs**-**GaAs** pseudomorphic heterostructure transistors prepd. by OMVPE technol., i.e. **InGaAs**-**GaAs** **graded**-concn. doping-**channel** MIS-like field effect transistors (FET) and heterostructure-emitter and heterostructure-base (**InGaAs**-**GaAs**) transistors (HEHBT). For the doping-channel MIS-like FET, the graded In0.15Ga0.85As doping-channel structure is employed as the active channel. For a 0.8.times.100 .mu.m2 gate device, a breakdown voltage of 15 V, a max. transconductance of 200 mS/mm, and a max. drain satn. current of 735 mA/mm were obtained. For the HEHBT, the confinement effect for holes is enhanced owing to the presence of **GaAs**/**InGaAs**/**GaAs** quantum wells. Thus, the emitter injection efficiency is increased and a high current gain can be obtained. Also, due to the lower surface recombination velocity of **InGaAs** base layers, the potential spike of the emitter-base (E-B) junction can be reduced significantly. This can provide a lower collector-emitter offset voltage. For an emitter area of 4.9 .times. 10-5 cm2, the common emitter current gain of 120 and the collector-emitter offset voltage of 100 mV were obtained.

L31 ANSWER 9 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:958762 HCAPLUS
DN 124:73900
TI Compound semiconductor **heterojunction** field-effect transistors
IN Ashizawa, Yasuo; Fujita, Shinobu; Amano, Minoru
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07249758	A2	19950926	JP 1994-41276	19940311

AB The channel layer in the FETs comprises a region in which forbidden band widenes from the source- toward drain sides. Barrier layer, next to the channel layer and having wider forbidden band than that of channel layer, in the FET comprises a region in which band uncontinuousness (from the channel layer) increases from the source- toward drain sides. The channel layer and barrier layer may be InxGa1-xAs, and In1-yAlyAs, resp. The FET inhibits depression of withstand even if using a compd. semiconductor having narrow forbidden band.

L31 ANSWER 10 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:66835 HCAPLUS
DN 120:66835
TI On the improvement of gate voltage swings in .delta.-doped **gallium arsenide**/indium **gallium arsenide**/ **gallium arsenide** pseudomorphic heterostructures
AU Hsu, Wei Chou; Shieh, Hir Ming; Kao, Ming Jer; Hsu, Rong Tay; Wu, Yu Huei
CS Dep. Electr. Eng., Natl. Cheng-Kung Univ., Tainan, Taiwan
SO IEEE Trans. Electron Devices (1993), 40(9), 1630-5
CODEN: IETDAI; ISSN: 0018-9383
DT Journal
LA English
AB Significant improvements on gate voltage swings in .delta.-doped **GaAs**/InxGa1-xAs/**GaAs** pseudomorphic heterostructures prepd. by low-pressure metalorg. chem. vapor deposition are demonstrated and discussed. Structure utilizing a compositionally **graded** InxGa1-xAs **channel** revealed a very flat transconductance region of 2 V. While the gate voltage swings of single and double .delta.-doped **GaAs**/In0.25Ga0.75As/**GaAs** structures were 2.5 and 2.8 V, resp. All structures in this work also exhibited high extrinsic transconductances as well as high satn. current densities.

L31 ANSWER 11 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:14595 HCAPLUS
DN 118:14595
TI Novel indium **gallium arsenide** (InyGa1-yAs)/ **gallium arsenide graded** superlattice **channel** (0.2 .ltoreq. y .ltoreq.0.4) for pseudomorphic AlxGa1-xAs/InyGa1-yAs HFET
AU Kraus, J.; Meschede, H.; Liu, Q.; Prost, W.; Tegude, F. J.; Lakner, H.; Kubalek, E.
CS Sonderforschungsber. 254, Univ.- GH - Duisburg, Duisburg, D-4100, Germany
SO Proc. - Electrochem. Soc. (1992), 92-20(Proc. State-of-the-Art Program Comd. Semicond., 16th, Symp. Mater. Process. Issues Large Scale Integr. Electron. Photonic Arrays, 1992), 112-21
CODEN: PESODO; ISSN: 0161-6374

DT Journal
LA English
AB MBE growth optimization, transport properties and rf-performance of pseudomorphic HFET incorporating a graded InyGa1-yAs/**GaAs** superlattice channel are reported.

D BIB AB 1-18 L38

L38 ANSWER 1 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:583351 HCAPLUS
DN 135:311492
TI Molecular beam epitaxial growth and characterization of strain-compensated Al0.3In0.7P/InP/Al0.3In0.7P metamorphic-pseudomorphic high electron mobility transistors on **GaAs** substrates
AU Hoke, W. E.; Lemonias, P. J.; Kennedy, T. D.; Torabi, A.; Tong, E. K.; Chang, K. L.; Hsieh, K. C.
CS Raytheon RF Components, Andover, MA, 01810, USA
SO J. Vac. Sci. Technol., B (2001), 19(4), 1519-1523
CODEN: JVTBD9; ISSN: 0734-211X
PB American Institute of Physics
DT Journal
LA English
AB A novel metamorphic high-electron-mobility transistor (HEMT) structure was grown on **GaAs** substrates by solid-source mol.-beam epitaxy for potential microwave power applications. The HEMT device layers were strain compensated with pseudomorphic (tensile-strained) Al0.3In0.7P donor-barrier layers and a pseudomorphic (compressive-strained) InP **channel layer**. At. force microscopy measurements of the metamorphic structure yielded a root-mean-square surface roughness of 8 .ANG.. Transmission electron micrographs of the device layers exhibited flat interfaces with the dislocation d. estd. to be less than 1 .times. 106 cm-2. Room temp. photoluminescence measurements of metamorphic AlInP layers indicated large direct **band gaps** up to 2.10 eV. Due to the larger conduction band discontinuity at the Al0.3In0.7P/InP **heterojunction** than the AlGaAs/**InGaAs** **heterojunction** in **GaAs** pseudomorphic HEMTs, significantly higher channel sheet densities were obtained. For Al0.3In0.7P/InP HEMTs, channel sheet densities exceeding 3 .times. 1012 cm-2 for single-pulse-doped, and greater than 4 .times. 1012 cm-2 for double-pulse-doped, structures were readily obtained. Hall measurements on a double-pulse-doped Al0.3In0.7P/InP/Al0.3In0.7P HEMT gave mobilities of 4450 and 18,500 cm2/V.cntdot.s at 300 and 77 K, resp., which are consistent with a high quality InP **channel layer**. Secondary ion mass spectroscopy depth profiles of a double-pulse-doped structure displayed sharp doping pulses and interfaces indicating that metamorphic growth was not leading to enhanced diffusion or migration. Initial and non-optimized devices with a gate length of 0.15 .mu.m exhibited a max. c.d. of 500 mA/mm and a transconductance of 520 mS/mm, which compare favorably to mature AlGaAs/**InGaAs** pseudomorphic HEMTs.
RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L38 ANSWER 2 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:185139 HCAPLUS
DN 134:230621
TI Field-effect semiconductor device with lowered series resistance
IN Inai, Makoto; Sasaki, Hidehiko
PA Murata Manufacturing Co., Ltd., Japan
SO Eur. Pat. Appl., 14 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1
PATENT NO. KIND DATE APPLICATION NO. DATE

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     --------------- ---- --------         --------------- --------
PI   EP 1083608       A1   20010314        EP 2000-119779   20000911
         R:  AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT,
             IE, SI, LT, LV, FI, RO
     JP 2001085672    A2   20010330        JP 1999-256059   19990909
PRAI JP 1999-256059   A    19990909
```

AB A field-effect semiconductor device including a **channel layer** (4); a contact layer (6); a semiconductor structure (5) having an electron-affinity different from those of the **channel layer** (4) and the contact layer (5) and formed between the **channel layer** (4) and the contact layer (5); an ohmic electrode (8,9) formed on the contact layer (6); and a Schottky electrode (10) formed on the semiconductor structure (5). The junction between the **channel layer** (4) and the semiconductor structure (5) and the junction between the contact layer (6) and the semiconductor structure (5) are isotype **heterojunctions**.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L38 ANSWER 3 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:622349 HCAPLUS
DN 131:222125
TI High frequency **heterojunction** type field effect transistor using multilayer electron feed layer
IN Niwa, Takaki
PA NEC Corporation, Japan
SO U.S., 21 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

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     PATENT NO.       KIND DATE            APPLICATION NO.  DATE
     --------------- ---- --------         --------------- --------
PI   US 5959317       A    19990928        US 1997-979177   19971126
     JP 10214962      A2   19980811        JP 1997-178471   19970703
     JP 3058262       B2   20000704
PRAI JP 1996-317627   A    19961128
     JP 1997-178471   A    19970703
```

AB A **heterojunction** type field effect transistor can control a short channel effect, reduce the fluctuation of a threshold, and improve a yield. The **heterojunction** type field effect transistor comprises: a semiconductor substrate, a 1st electron feed layer made of a doped semiconductor having a wider **band gap** than the **channel layer**, a **channel layer** made of a nondoped semiconductor, a 2nd electron feed layer comprising a laminate structure of a plurality of semiconductor layers having a wider **band gap** than the **channel layer** and having a thickness of 100 .ANG. or less, and a gate electrode, a source electrode, and a drain electrode.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L38 ANSWER 4 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:34541 HCAPLUS
DN 130:89337
TI High power HFET with improved channel interfaces
IN Wang, Yang; Hashemi, Majid M.; Eisenbeiser, Kurt; Huang, Jenn-Hwa
PA Motorola, Inc., USA
SO U.S., 6 pp.

CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5856684	A	19990105	US 1996-712760	19960912

AB A high power **heterojunction** field effect transistor comprises a 1st barrier layer including a semiconductor material having a **band gap**, a 2nd barrier layer including a semiconductor material having a **band gap**, a **channel layer** including a semiconductor material having a **band gap** narrower than the **band gaps** of the material included in the 1st barrier layer and the 2nd barrier layer and sandwiched there between and an interface **layer** sandwiched between the **channel layer** and the 1st barrier layer.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L38 ANSWER 5 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:394990 HCAPLUS
DN 129:182529
TI Preparation and properties of edge QW delta doped **InGaAs/GaAs** FET
AU Bujdak, M.; Lalinsky, T.; Harman, R.; Kostic, I.; Hudek, P.; Nemeth, S.
CS Dept. of Microelectronics, Slovak Technical University, Bratislava, 812 19, Slovakia
SO NATO Sci. Ser., 3 (1998), 48(Heterostructure Epitaxy and Devices - HEAD'97), 255-258
CODEN: NSSTFF
PB Kluwer Academic Publishers
DT Journal
LA English
AB Doped **channel heterojunction** FET (HFET) **layer** structure was grown by MBE on semi-insulated (100) **GaAs** substrate. It consists of the undoped **GaAs** buffer layer 500 nm thick followed by undoped strained In0.2Ga0.8As **channel layer** and top **GaAs Schottky contact**. The growth was completed by highly doped **GaAs** cap layer in order to reduce the resistance of access region and ohmic contacts.

L38 ANSWER 6 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:49018 HCAPLUS
DN 128:161443
TI High-performance heterostructure field-effect transistors (HFETs) with step-modulated **InGaAs** channel structure
AU Liu, Wen-Chau; Laih, Lih-Wen; Chang, Wen-Lung; Cheng, Shiou-Ying
CS Department of Electrical Engineering, National Cheng-Kung University, Tainan, Taiwan
SO Mater. Chem. Phys. (1998), 52(1), 89-93
CODEN: MCHPDR; ISSN: 0254-0584
PB Elsevier Science S.A.
DT Journal
LA English
AB Two types of new heterostructure field-effect transistors, i.e., a SDCFET (step-doped channel field-effect transistor) and a SCDCFET (step-compositioned doped channel field-effect transistor), are fabricated and investigated in this paper. The pseudomorphic InxGa1-xAs (x .ltoreq. 0.2) and Al0.3Ga0.7As (or In0.49Ga0.51P) layers are used as the active

channel and **Schottky contact layer**, resp., in these studied devices. Owing to the large conduction band discontinuity (.DELTA.EC) at InxGa1-xAs/Al0.3Ga0.7As and InxGa1-xAs/In0.49Ga0.51P interfaces, the carriers can be easily confined in the channels. Thus the device characteristics such as drain satn. current, breakdown voltage and transconductance (gm) are improved. Furthermore, by varying the doping concn. or In compn. in the channel, both the high carrier d. and high output current may be obtained as a result of the significant carrier accumulation effect. From the exptl. results, these studied devices show their great potential in high-power and high-speed circuit applications.

L38 ANSWER 7 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:800843 HCAPLUS
DN 128:108909
TI Millimeter-wave power HEMTs
AU Arai, Shigemitsu; Tokuda, Hirokuni
CS Microwave Solid-State Department, Komukai Works, Toshiba Corporation, Kawasaki, 210, Japan
SO Solid-State Electron. (1997), 41(10), 1575-1579
CODEN: SSELA5; ISSN: 0038-1101
PB Elsevier Science Ltd.
DT Journal; General Review
LA English
AB A review with 4 refs. The performance of millimeter-wave PM-HEMAT and HEFT are compared. There are two structures in the millimeter-wave **heterojunction** FETs. One is a HEMT, mainly Pseudomorphic **InGaAs** HEMT (PE-HEMT) and the other is a **Heterojunction** FET (HFET), which uses an n-AlGaAs and an n-**InGaAs** or **GaAs** layer as a **Schottky contact** and **channel layer**, resp. Although a PM-HEMT is superior to HFET in terms of gain and higher operating frequency, it tends to be lower breakdown voltage. Therefore, the two devices were used according to the required output power and operating frequencies. This article describes the comparison of the structures and performances between HFET and PM-HEMT, then power performances of the devices developed in Toshiba are demonstrated.

L38 ANSWER 8 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:701909 HCAPLUS
DN 127:354364
TI Double-**heterojunction** field-effect transistor
IN Suzuki, Toshifumi; Ishikawa, Yamato
PA Honda Giken Kogyo Kabushiki Kaisha, Japan
SO Eur. Pat. Appl., 9 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 802570	A2	19971022	EP 1997-105136	19970326
	EP 802570	A3	19980805		
	R: DE, FR, GB				
	JP 09283746	A2	19971031	JP 1996-120974	19960418
	US 5900653	A	19990504	US 1997-839743	19970415
PRAI	JP 1996-120974		19960418		

AB A field-effect transistor has a double-**heterojunction** structure including a **channel layer** of **InGaAs** and

upper and lower wide-**band-gap** layers, esp. of Al0.2-0.3Ga0.7-0.8As, disposed resp. over and under the **channel layer** and each forming a **heterojunction** with the **channel layer**. The **channel layer** has such a thickness as to develop a substantially single electron gas **layer** in the **channel layer**. The upper and lower wide-**band-gap** layers have substantially the same impurity concn. The upper and lower wide-**band-gap** layers include doped planar layers positioned vertically sym. with respect to the **channel layer** and doped at the same concn.

L38 ANSWER 9 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:617873 HCAPLUS
DN 127:313752
TI **Heterojunction** field-effect transistors with an increased normal-directional withstand voltage
IN Hara, Naoki; Kuroda, Shigeru
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09246525	A2	19970919	JP 1996-47736	19960305

AB The title FETs comprise a substrate, a Group IIIA-VA compd. semiconductor **channel layer** formed on the substrate, an AlGaAs lower **Schottky contact layer** provided on the **channel layer**, an AlGaAs upper **Schottky contact** layer whose Al compn. smaller than that in the lower **Schottky contact** layer, a gate electrode provided on a portion of the upper **Schottky contact**, and a pair of current electrodes formed across the gate electrode each other and ohmic-contacted on the **channel layer**. The arrangement gives the FETs increased normal-directional withstand voltage between the gate and the source.

L38 ANSWER 10 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:301254 HCAPLUS
DN 124:330163
TI Semiconductor devices having **hetero-junction** bipolar transistors and fabrication thereof
IN Imamura, Kenichi
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08064612	A2	19960308	JP 1994-195458	19940819

AB The bipolar transistors in the title devices comprise a collector layer, a base electrode formed on the collector, and a pl. no. of emitters formed on the base layer. The base layer is not connected by electrodes. The transistors employs (1) the material for the base layer whose energy **band gap** is increased from the collector side to the emitter side, (2) the dopant concn. for the collector layer to be higher

towards the base layer, or (3) the thickness for the base layer so that the time for the carrier passing through the base from the emitter to collector is shorter than that for electron-hole recombination in the base layer. The arrangement gives the transistors a decreased current leakage, increased electron mobility, and simplified circuit structure.

L38 ANSWER 11 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:910557 HCAPLUS
DN 124:73881
TI Manufacture of **heterojunction** FETs
IN Negishi, Hitoshi
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07193223	A2	19950728	JP 1993-330334	19931227

AB In the manuf., comprising successively epitaxial growth of, on semi-insulating **GaAs** substrate; (a) **GaAs** buffer layer , (b) AlxGa1-xAs (0 < x < 1) heterobuffer layer, (c) InyGa1-yAs (0 < y < 1) **channel layer** of smaller **band gap** than (b), and (d) AlzGa1-zAs (0 < z < 1) electron-donating layer of larger **band gap** than (c); substrate temp. at 600-700.degree. is applied for growing (a) and (d), and at 400-500.degree. for (b) and (c). Manuf. of FETs with x = y = z = 0.2 is also claimed.

L38 ANSWER 12 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:863537 HCAPLUS
DN 123:273557
TI **Heterojunction** FET's
IN Haruyama, Junshi
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07153937	A2	19950616	JP 1993-300257	19931130
	JP 2581423	B2	19970212		

AB The FET has a undoped (Ga,In)As channel (e.g., 20% in In ratio and 150 .ANG. thick), a 1st Si-doped **GaAs** (e.g., 50 .ANG. thick and 3 .times. 1018 cm-3 in Si concn.), a Si-doped (Al,Ga)As, an undoped (Al,Ga)As (e.g., 200 .ANG. thick), a 2nd Si-doped **GaAs** layer sequentially formed on a semiconductor substrate, and a gate electrode in **Schottky contact** on the undoped (Al,Ga)As layer, and the source and the drain electrode in ohmic contact on the 2nd **GaAs** layer. The FET has increased gate-voltage resistance and retains linear gains in driving at large signals.

L38 ANSWER 13 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:643663 HCAPLUS
DN 123:45963
TI **Heterojunction** field-effect transistor
IN Haruyama, Junshi

PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07074347	A2	19950317	JP 1993-171095	19930617
	JP 2500457	B2	19960529		

AB The title transistor consists of the following layers: (1) a barrier layer having a 1st **band gap**, (2) non-doped 1st **channel layer** having a 2nd **band gap** which is narrower than the 1st **band gap**, (3) a doped 1st electron-supplying layer having a 3rd **band gap** which is narrower than the 1st **band gap** and wider than the 2nd **band gap**, (4) a non-doped 2nd **channel layer** having a narrower **band gap** than the 3rd **band gap**, (5) a non-doped 2nd electron-supplying layer having a wider **band gap** than the 3rd **band gap**, and (6) a gate electrode which from Schottky-junction. The 2nd electron-supplying layer may be AlGaAs. The **channel layer** may be **InGaAs**. The 1st electron-supplying layer may be **GaAs**. The transistor has a high electron mobility even in a high frequency region.

L38 ANSWER 14 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:408416 HCAPLUS
DN 122:176452
TI Schottky **hetero-junction** field-effect transistors
IN Enoki, Takatomo; Kobayashi, Takashi; Ida, Minoru
PA Nippon Telegraph & Telephone, Japan
SO Jpn. Kokai Tokkyo Koho, 16 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06216160	A2	19940805	JP 1993-19678	19930112
	JP 3120611	B2	20001225		

AB **Channel layers** (e.g., **InGaAs**), carrier-supplying layers (e.g., InAlAs), etching stopper layers, **Schottky contact** layers (e.g., InAlAs) are successively laminated on semiconductor substrates (e.g., InP), gate electrodes (e.g., WSi) are formed on the laminated layers, insulator films are formed on the side of the electrodes, the **Schottky contact** layers are etched with the ate electrodes and the insulator films as masks to create **Schottky contacts** with the gate electrodes.

L38 ANSWER 15 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:151068 HCAPLUS
DN 120:151068
TI **Heterojunction** field effect transistor
IN Nakajima, Shigeru
PA Sumitomo Electric Industries, Ltd., Japan
SO Eur. Pat. Appl., 14 pp.
CODEN: EPXXDW
DT Patent

LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 562551	A2	19930929	EP 1993-104761	19930323
	EP 562551	A3	19931201		
	R: DE, DK, FR, GB, SE				
	JP 05267351	A2	19931015	JP 1992-64831	19920323
	JP 05267352	A2	19931015	JP 1992-64833	19920323
	JP 3233167	B2	20011126		
	CA 2091926	AA	19930924	CA 1993-2091926	19930318
	US 5446296	A	19950829	US 1995-383653	19950203
PRAI	JP 1992-64831	A	19920323		
	JP 1992-64833	A	19920323		
	US 1993-31965	B1	19930316		

AB In this metal-semiconductor FET, an undoped AlInAs layer, an undoped InP layer, an n-**InGaAs** layer, an undoped InP layer, and an AlInAs layer are formed on a semi-insulating InP substrate. A **source electrode**, a **drain electrode**, and a gate electrode are formed on the AlInAs layer. The **source electrode** and the **drain electrode** are in ohmic contact with the AlInAs layer, and the gate electrode forms a Schottky junction with the AlInAs layer.

L38 ANSWER 16 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:97257 HCAPLUS
DN 116:97257
TI **Heterojunction** field-effect transistors and manufacturing thereof
IN Matsumoto, Fumio; Nakano, Haruo
PA Sanyo Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 03070145	A2	19910326	JP 1989-207613	19890809

AB The title transistor is provided by successive lamination on a semiconductor by an electron donor **layer**, a **channel layer**, and a **barrier layer**, wherein the forbidden band width for the electron donor **layer** and the **barrier layer** is wider than that of the **channel layer**. The title manufg. involves (1) depositing a nondoped **GaAs** spacer layer on the electron donor layer and (2) subsequently depositing a nondoped **InGaAs channel layer** and a nondoped **GaAs barrier layer** successively on the spacer layer. The arrangement gives a low-resistance and stable ohmic contact and high-quality Schottky characteristics.

L38 ANSWER 17 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:462133 HCAPLUS
DN 115:62133
TI Transport properties of heterostructures based on gallium antimonide, indium arsenide and indium antimonide on **gallium arsenide** substrates
AU Uppal, P. N.; Gill, D. M.; Svensson, S. P.; Cooke, D. C.
CS Martin Marietta Lab., Baltimore, MD, 21227-3898, USA

SO J. Cryst. Growth (1991), 111(1-4), 623-7
CODEN: JCRGAE; ISSN: 0022-0248
DT Journal
LA English
AB Heterostructures were grown based on low **band-gap** channels of GaxIn2-xSb (x = 0.5) and InAsxSb1-x (x = 0.4-1) alloys. For barrier layers, AlxIn1-xSb (x = 1-0.5) with a compn. chosen to be closely lattice matched to the **channel layers**, GaxIn1-xSb and InAsxSb1-x were grown. A AlxGa1-xAs/GaAsySb1-y/**GaAs** pseudomorphic heterostructure was grown which is an analog of the InxGa1-xAs pseudomorphic MODFET. In the case of AlxIn1-xSb/GaxIn1-xSb and AlxIn1-xSb/InAsxSb1-x heterostructures, the barrier layers were undoped but one obsd. 2-dimensional electron densities of .apprx.7 x 1011 to 2 x 1012 cm-2 at 300 K. For the AlSb/InAs and Al0.7In0.3Sb/Ga0.7In0.3Sb heterostructures, the 300 K mobilities are 24,000 and 3000 cm2/V.s, resp. Mobilities for the AlxIn1-xSb/InAsxSb1-x heterostructures are .apprx.12,000 cm2/v.s. Hall measurements on the AlxGa1-xAs/GaAsySb1-y/ **GaAs** heterostructures indicated 2D-electron densities of 3 x 1012 cm-2 and mobilities of 3,000 cm2/V.s.

L38 ANSWER 18 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:28751 HCAPLUS
DN 112:28751
TI Band-**edge** discontinuities of strained-**layer** indium gallium **heterojunctions** and quantum wells
AU Niki, S.; Lin, C. L.; Chang, W. S. C.; Wieder, H. H.
CS Dep. Electr. Comput. Eng., Univ. California, San Diego, La Jolla, CA, 92093, USA
SO Appl. Phys. Lett. (1989), 55(13), 1339-41
CODEN: APPLAB; ISSN: 0003-6951
DT Journal
LA English
AB The conduction-band discontinuity (.DELTA.Ec) and the **band-gap** offset (.DELTA.Egh) of InxGa1-xAs/**GaAs** multiple quantum wells grown on **GaAs** substrates by mol. beam epitaxy are investigated for 0 < x < 0.3. The **band gap** of strained InxGa1-xAs, detd. from the excitonic transition of room-temp. transmission spectra, is found to be linearly dependent on x and is in good agreement with the calcd. values. The **band-gap** offset is found to be .DELTA.Egh = 1.15x eV. The conduction-band offset, compiled from published data, is .DELTA.Ec = 0.75x eV, and thus (.DELTA.Ec/.DELTA.Egh) = 0.65 independent of x.

=> D BIB AB L41 1-2

L41 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:311375 HCAPLUS
DN 124:330149
TI **Heterojunction** FETs
IN Yoshida, Naoto; Uneme, Yutaka
PA Mitsubishi Electric Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08064807	A2	19960308	JP 1994-200945	19940825

AB The transistors contain semi-insulating InP substrates, undoped AlInAs buffer layers, i-InxGa1-xAs low-concn. channel layers, i-InyGa1-yAs high-concn. channel layers, undoped AlInAs Schottky-forming **layers**, n-**InGaAs contact layers**, source and **drain electrodes**. Current runs between the source and **drain electrodes** through 2-dimensional electron gases formed at the interface of the 2 channel layers, decreasing noise.

L41 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:562177 HCAPLUS
DN 117:162177
TI **Heterojunction** semiconductor device
IN Aoki, Yoshio
PA Fujitsu K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04064240	A2	19920228	JP 1990-179001	19900704

AB A **heterojunction** semiconductor device has (1) an n cond.-type 1st semiconductor layer (e.g., **GaAs**, AlGaAs), (2) a 2nd semiconductor layer (e.g., **InGaAs**, **GaAs**) which on the 1st semiconductor layer, contains an n cond.-type impurity at near the interface, (3) a 3rd semiconductor layer (e.g., AlGaAs) which on the 2nd semiconductor layer, is virtually free of an impurity, (4) source, drain, and gate electrodes selectively formed on the 3rd semiconductor **layer**, and (5) **contact** regions beneath the source and **drain electrodes**, reaching the semiconductor layer, resp. This **heterojunction** semiconductor device is characterized in that an electron affinity of the 3rd semiconductor layer is smaller than that of the 1st semiconductor layer and an electron affinity of the 1st semiconductor layer is smaller than that of the 2nd semiconductor layer. This **heterojunction** semiconductor device with an uncontrolled dopant regions does not give inferior device characteristics.

=> D BIB AB L43 1-12

L43 ANSWER 1 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:745907 HCAPLUS
DN 135:296008
TI Semiconductor light-emitting devices and manufacture
IN Kawazura, Eiji; Kikugawa, Tomoyuki; Shinone, Katsunori
PA Anritsu Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001284735	A2	20011012	JP 2000-98194	20000331

AB The devices comprise: (1) an n electrode; (2) an n-InP substrate; (3) an n-GaInAsP marker, (4) an n-InP 1st cladding, and (5) an n-GaInAs etch stop layer; a mesa comprising (6) an n-InP 2nd cladding, (6) a MQW active, (7) a p-InP 3rd cladding and (8) a p-GaInAsP cap layer; (9) an n-InP **block layer** having a central aperture opening; (10) a p-InP **contact layer** burying (9); and a p electrode.

L43 ANSWER 2 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:749225 HCAPLUS
DN 133:303244
TI Semiconductor laser devices
IN Anayama, Shinji
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000299531	A2	20001024	JP 1999-108770	19990416

AB The devices comprise: an n-**GaAs** substrate having an inclined step [(100) toward (111)A]; an n-**GaAs** buffer, an n-AlGaAs cladding, and a GaInAs-QW/**GaAs-barrier** MQW active **layer**; an n-GaInP current **block layer** (.dblvert. (111)) having a p-GaInP layer in the inclined region (.dblvert. (311)); and a p- AlGaAs cladding and a p-**GaAs contact layer**.

L43 ANSWER 3 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:512039 HCAPLUS
DN 133:112234
TI Semiconductor laser devices and manufacture
IN Kinoshita, Junichi
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI JP 2000208872 A2 20000728 JP 1999-5604 19990112
AB The devices comprise: an n electrode; an n-**GaAs** substrate; an n-AlGaAs cladding **layer**; an AlAs-**barrier**/AlGaAs-well (or AlInAs barrier/GaInAsP-well) MQW active layer; a p-AlGaAs cladding layer; a Zn (or B) diffused disordered AlAs/AlGaAs superlattice current-aperture layer; an oxidized AlAs/AlGaAs superlattice high-resistance current-**confinement layer**; a p-**GaAs contact layer**; and a p electrode.

L43 ANSWER 4 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:611007 HCAPLUS
DN 131:235527
TI Surface-emitting semiconductor lasers and their manufacture
IN Iwai, Norihiro; Mukaihara, Tomokazu
PA Furukawa Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11261157	A2	19990924	JP 1998-65149	19980316

AB The lasers comprise **GaAs** substrates, **GaAs**/Al(Ga)As multilayer reflection mirrors, post-like active layers embedded by InP-type compd. semiconductors current-**blocking layers**, and reflection mirrors of dielec. films. The lasers are manufd. by (1) forming laminates having double-**heterojunction** structures contg. active layers on InP substrates, (2) etching the active layers to give post-like active layers, (3) embedding the active **layers** by current-**blocking layers**, (4) removing the InP substrates, (5) forming **GaAs**/Al(Ga)As multilayer reflection mirrors on **GaAs** substrates, (6) bonding the reflection mirrors with the laminates, and (7) forming reflection mirrors on the laminates. The lasers show low threshold current and low working voltage.

L43 ANSWER 5 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:421251 HCAPLUS
DN 129:115402
TI Manufacture of semiconductor laser devices
IN Senda, Hiroaki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10173278	A2	19980626	JP 1996-332207	19961212
	JP 3147148	B2	20010319		

AB The devices comprise: (1) an n-substrate; (2)/(3) a 1st and a 2nd n-cladding layer; (4) an n-etch stop layer; (5)/(6) a 3rd n-cladding and a n-guide layer; (7) a GaInAs-well/**GaAs-barrier** active **layer**; (8)/(9) a p-guide and a 1st p-cladding layer; (10) a p-etch stop layer; (11)/(12) a 2nd and a 3rd cladding layer; (13) a p-**GaAs** cap layer; (14)/(15)a 1st and a 2nd n-current **block layer**; (16) a p-**contact layer**; (17) a TiPtAu p-electrode; and (18) a AuGeNi n-electrode, where (1), (13), (15) and (16)

employ **GaAs**; (2)-(6), (8)-(12), and (14) comprise AlGaAs; and the fabrication comprises a wet and a dry etching selectively.

L43 ANSWER 6 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:1365 HCAPLUS
DN 128:83272
TI Structure of the heterostructure-emitter and heterostructure-base transistor (HEHBT)
IN Liu, Wen-chau; Lour, Wen-shiung; Tsai, Jung-hui
PA National Science Counsel of Republic of China, Taiwan
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5698862	A	19971216	US 1996-766711	19961213

AB The invention presents a structure of heterostructure-emitter and heterostructure-base transistor. The device structure are, from bottom upward in succession, a substrate, a buffer layer, a collector layer, a base layer, a quantum well, an emitter **layer**, a **confinement layer** and an ohmic **contact layer**. Of them, except the quantum well which is made of **InGaAs** and the **confinement layer** which is formed by AlGaAs, the rest are all made of **GaAs** material. Base on the design of the heterostructure of base and emitter, a transistor of such structure, under normal operation mode, possesses high-current gain and low-offset voltage so as to reduce undesirable power consumption. In addn., under the inverted operation mode, the interesting multiple S-shaped neg.-differential-resistance (NDR) may be obtained due to the avalanche multiplication and two-stage carrier confinement effects. These properties cause the device of the invention to provide good promise for amplification, oscillator, and multiple-valued logic circuits applications.

L43 ANSWER 7 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:240119 HCAPLUS
DN 126:232352
TI Ohmic contact structure, semiconductor device with it, and its manufacture
IN Yakura, Mototsugu; Sato, Hiroya
PA Sharp Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09045890	A2	19970214	JP 1996-125159	19960520
	US 6188137	B1	20010213	US 1996-652303	19960523
PRAI	JP 1995-126911	A	19950525		
	JP 1996-125159	A	19960520		

AB The structure comprises successively laminated layers of InxGa1-xAs (0 < x .ltoreq. 1), Pt or Pd, and .gtoreq.1 metal layer. The semiconductor device contg. a pn **hetero-junction**, includes .gtoreq.1 the contact structure on p- and n-type semiconductor layers, resp. The device is manufd. by these steps; successively depositing Pt or Pd layers and .gtoreq.1 metal layers on p- and n-type semiconductor layers, resp.,

and patterning. The device shows low contact resistance even under high-temp. annealing and low cost.

L43 ANSWER 8 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:667423 HCAPLUS
DN 126:96470
TI Double injection and negative resistance in stripe-geometry oxide-aperture AlyGa1-yAs-**GaAs**-InxGa1-xAs quantum well heterostructure laser diodes
AU Wierer, J. J.; Maranowski, S. A.; Holonyak, N., Jr.; Evans, P. W.; Chen, E. I.
CS Elec. Eng. Res. Lab., Univ. of Illinois, Urbana, IL, 61801, USA
SO Appl. Phys. Lett. (1996), 69(19), 2882-2884
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB Data are presented demonstrating double injection and neg. resistance in stripe-geometry oxide-aperture AlyGa1-yAs-**GaAs**-InxGa1-xAs quantum well heterostructure lasers. The buried oxide laser structures are defined, in current and cavity, by laterally oxidizing the higher Al compn. upper and lower cladding layers from mesa edge (a ridge), thus, forming a narrow oxide-defined buried aperture (.apprx.2 .mu.m). Post fabrication annealing (425.degree. in N2) removes the neg. resistance, indicating that the crystal growth and oxidn. processes introduced products such as H and OH in the active region that compensate the dopants.

L43 ANSWER 9 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:997145 HCAPLUS
DN 124:19894
TI Field-effect transistor and manufacture thereof
IN Matsumoto, Hidetoshi; Hiruma, Takeyuki
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07263664	A2	19951013	JP 1994-46718	19940317

AB A Group III-V compd. semiconductor field-effect transistor, wherein the **heterojunction barrier layer** is formed in the **contact layer** situated above the channel layer.

L43 ANSWER 10 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:910556 HCAPLUS
DN 123:356723
TI Field-effect transistors
IN Matsunaga, Takaharu
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI JP 07193222 A2 19950728 JP 1993-333432 19931227
AB In an AlGaAs/(In)**GaAs** type-**heterojunction** FET, and AlAs hole **barrier layer** is comprised in the AlGaAs spacer layer. The FET of above structure comprises 2 ohmic **contact layers** of **GaAs** with high- and low-concn. n-type dopant. The FET reduces gate leak current and hole generation below the gate.

L43 ANSWER 11 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:437866 HCAPLUS
DN 117:37866
TI Growth of **gallium arsenide**/aluminum **gallium arsenide HBTs** by MOMBE (CBE)
AU Abernathy, C. R.; Ren, F.; Pearton, S. J.; Fullowan, T. R.; Montgomery, R. K.; Wisk, P. W.; Lothian, J. R.; Smith, P. R.; Nottenburg, R. N.
CS AT and T Bell Lab., Murray Hill, NJ, 07974, USA
SO J. Cryst. Growth (1992), 120(1-4), 234-9
CODEN: JCRGAE; ISSN: 0022-0248
DT Journal
LA English
AB The unique growth chem. of MOMBE, which can be used to produce high speed **GaAs**/AlGaAs **heterojunction** bipolar transistors (**HBTs**), is described.. The ability to grow heavily doped, well-**confined layers** with C doping from trimethylgallium (TMG) is a significant advantage for this device. In addn. to high p-type doping, high n-type doping is also required. While elemental Sn can be used to achieve doping levels up to 1.5 .times. 1019 cm-3, severe segregation limits its use to surface **contact layers**. With tetraethyltin (TESn), however, segregation does not occur and Sn doping can be used throughout the device. Using these sources along with triethylgallium (TEG), trimethylamine alane (TMAA), and AsH3, a Npn device was fabricated.

L43 ANSWER 12 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:164229 HCAPLUS
DN 116:164229
TI Semiconductor device
IN Imamura, Kenichi
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 03080543	A2	19910405	JP 1989-215948	19890824
	JP 2808145	B2	19981008		

AB A 1st semiconductor device comprises a collector-**contact** (n-**InGaAs**) **layer** on a substrate, a collector (n-InP) layer on part of the collector-**contact layer**, a base (p-**InGaAs**) having an overhang structure on the collector layer, and an emitter (n-InAlAs) layer on the base layer (corresponding to the collector layer). A 2nd semiconductor device comprises a collector (n-**InGaAs**) layer on a substrate, a collector-**barrier** (i-InP) **layer** on part of the collector layer, a base (n-**InGaAs**) layer having an overhang structure on the collector-**barrier layer**, an emitter-**barrier** on the base layer (corresponding to the collector-**barrier layer**),

and an emitter (n-**InGaAs**) layer on the emitter-**barrier layer**. The above semiconductor devices are useful as a **heterojunction** bipolar transistor, hot-electron transistor, or resonant tunneling hot-electron transistor having a decreased base-collector junction capacitance.

=> D BIB AB 1-3

L44 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:656358 HCAPLUS
DN 125:290581
TI p-Type field effect semiconductor devices and complementary field effect semiconductor devices and manufacture thereof
IN Harada, Naoki
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08213559	A2	19960820	JP 1995-16594	19950203

AB The p-type field effect device has a heterojunction from a Ga(As,Sb) layer and a 2nd p-type semiconductor layer (e.g., InP) having the upper limit of the valency electron band lower than that of the Ga(As,Sb) layer, and a Schottky electrode on the side of the surface from the 2nd semiconductor layer for change of thickness of a depletion layer and change of 2-dimensional pos. hole gas concn. accumulated on the side of the Ga(As,Sb) layer of the heterojunction, and the complementary field effect device which has the channel layer from (Ga,In)As, InP, Ga(As,Sb), or In(As,P), and the electron supply layer from n-(Al,In)As, n-(Al,Ga,In)As, or n-InP on the same substrate.

L44 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:93021 HCAPLUS
DN 120:93021
TI Quantum well p-channel field-effect transistor, and integrated circuit having complementary transistors
IN Nuyen, Linh T.; Castagne, Jean
PA Picogiga S. A., Fr.
SO PCT Int. Appl., 35 pp.
CODEN: PIXXD2
DT Patent
LA French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9315523	A1	19930805	WO 1993-FR61	19930121
	W: JP, US				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	FR 2686455	A1	19930723	FR 1992-668	19920122
	FR 2694132	A1	19940128	FR 1992-8985	19920721
	FR 2694132	B1	19941014		
	EP 623244	A1	19941109	EP 1993-904106	19930121
	R: DE, FR, GB, NL				
	JP 07506461	T2	19950713	JP 1993-512972	19930121
PRAI	FR 1992-668		19920122		
	FR 1992-8985		19920721		
	WO 1993-FR61		19930121		

AB A transistor comprises an AlxGa1-xAs (or AlxIn1-xAs) layer and a GayIn1-yAs layer defining, at the latter layer, a quantum well having HH-type sub-bands. The thickness of the GayIn1-yAs layer is selected so that when a neg. voltage (VG) is applied to the gate, sub-bands HH1, HH2,

HH3,... occur in the quantum well and are sepd. by sufficient energy to ensure that the sub-bands corresponding to the highest effective masses M*h// have a substantially lower hole d. than sub-band HH1, whereby a hole build-up condition is created in the quantum well and the transconductance of the component is correlatively increased. This corresponds to a GayIn1-yAs thickness of about 4-6 nm for 25-35% In, or 6-9 nm for 25-30% In. In order to further improve performance, a ternary structure such as AlxGa1-xAs/GayIn1-yAs/AlzGa1-zAs, AlxGa1-xAs/GaAswSb1-w/AlzGa1-zAs or AlxGa1-xAs/GayIn1-yAswSb1-w/AlzGa1-zAs may also be provided.

L44 ANSWER 3 OF 3 HCAPLUS
AN 1988:520551 HCAPLUS
DN 109:120551
TI Study of molecular-beam epitaxy of gallium arsenide antimonide (GaAs1-xSbx) (x < 0.76) grown on gallium arsenide(100)
AU Zhao, J. H.; Li, A. Z.; Jeong, J.; Wong, D.; Lee, J. C.; Milliman, M. L.; Schlesinger, T. E.; Milnes, A. G.
CS Dep. Electr. Comput. Eng., Carnegie Mellon Univ., Pittsburgh, PA, 15213, USA
SO J. Vac. Sci. Technol., B (1988), 6(2), 627-30
CODEN: JVTBD9; ISSN: 0734-211X
DT Journal
LA English
AB Lattice-mismatched 0.5 to 1-.mu.m-thick GaAs1-xSbx epilayers were grown on (100) n-type GaAs by MBE throughout the whole compn. range and characterized for Sb content up to 0.76. The Sb incorporation coeff. is 0.42 at a substrate temp. of 480.degree.C. The epilayer quality was examd. by x-ray diffraction, photoluminescence, and photoresponse. The relationship between energy band gap of GaAs1-xSbx and Sb content at room temp. agrees with the result of R. Nahory et al. (1977) and that at 77 K is established and can be reasonably described by the estd. one from the binary band gaps of GaAs and GaSb at 77 K and the ternary band gaps of GaAs1-xSbx at 300 K. Both majority electron and hole traps in GaAs1-xSbx epilayers were characterized.

L49 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:384597 HCAPLUS
DN 132:355749
TI High-efficiency heterostructure thermionic coolers and their fabrication
IN Shakouri, Ali; Bowers, John E.
PA The Regents of the University of California, USA
SO PCT Int. Appl., 35 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000033354	A2	20000608	WO 1999-US27284	19991117
	WO 2000033354	A3	20010531		
	W: JP				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	EP 1131842	A2	20010912	EP 1999-969602	19991117
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI				
PRAI	US 1998-109342	P	19981120		
	WO 1999-US27284	W	19991117		

AB A heterostructure thermionic cooler and a method for making thermionic coolers, employing a barrier layer of varying conduction band edge for n-type material, or varying valence band edge for p-type material, that is placed between two layers of material. The barrier **layer** band **edge** is at least kBT higher than the Fermi level of the semiconductor layer, which allows only selected, hot electrons, or electrons of high enough energy, across the barrier. The barrier layer is constructed to have an internal elec. field such that the electrons that make it over the initial barrier are assisted in travel to the anode. Once electrons drop to the energy level at the anode, they lose energy to the lattice, thus heating the lattice of the anode. The barrier height of the barrier layer is high enough to prevent the electrons from traveling in the reverse direction.

L49 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:113324 HCAPLUS
DN 114:113324
TI Heterstructure device and production method thereof
IN Takikawa, Masahiko
PA Fujitsu Ltd., Japan
SO Eur. Pat. Appl., 16 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 397148	A2	19901114	EP 1990-108744	19900509
	EP 397148	A3	19910515		
	EP 397148	B1	19950104		
	R: DE, FR, GB				
	JP 02295136	A2	19901206	JP 1989-115135	19890510
	JP 2873583	B2	19990324		
	US 5170230	A	19921208	US 1990-521404	19900510
	US 5104825	A	19920414	US 1991-729998	19910715

PRAI JP 1989-115135 19890510
US 1990-521404 19900510

AB A semiconductor device includes an InP substrate, an intrinsic **InGaAs channel layer** formed on and lattice matched to the InP substrate, a doped **GaAsSb** carrier supply layer formed on the intrinsic **InGaAs channel layer** and lattice matched to the InP substrate, a 1st gate electrode formed on the doped **GaAsSb** carrier supply layer, and a 1st source electrode and a 1st drain electrode which are resp. formed on the doped **GaAsSb** carrier supply layer and located on both sides of the 1st gate electrode. A method involving etching for producing the device is described.

L55 ANSWER 1 OF 1 HCAPLUS
AN 1993:31514 HCAPLUS
DN 118:31514
TI Semiconductor device having an indium **gallium arsenide heterojunction**
IN Nakajima, Shigeru; Hayashi, Hideki
PA Sumitomo Electric Industries, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04214636	A2	19920805	JP 1990-401614	19901212

AB The device has a **heterojunction** of GaAsxSb1-x and InyGa1-yAs (x = 0.65-0.85; y = 0.3-0.65). The device showed high drain current and good **Schottky** characteristics.

L62 ANSWER 1 OF 1 HCAPLUS
AN 1993:181334 HCAPLUS
DN 118:181334
TI High-electron-mobility transistors
IN Harada, Naoki
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04214635	A2	19920805	JP 1990-70001	19900320

AB A high-electron-mobility transistor contains: (1) an **InP** substrate; (2) an undoped **InAsP channel layer** ; (3) an N-type InAlAs electron-supplying layer; (4) source and drain electrodes; and (5) a gate electrode on the electron-supplying layer between the source and drain electrodes, where the thickness of the **channel layer** is thinner than the crit. thickness for which dislocations are formed in crystals, and the d. of a 2-dimensional electron gas created in the **channel layer** is controlled by the application of voltage on the gate electrode.

D BIB AB 1-2

L67 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:707983 HCAPLUS
DN 123:126199
TI Photoluminescence study of **band-gap** alignment of intermixed **InAsP**/InGaAsP superlattices
AU Francis, C.; Boucaud, P.; Julien, F. H.; Emery, J. Y.; Goldstein, L.
CS Inst. d'Electronique Fondamentale, Univ. Paris XI, Orsay, 91405, Fr.
SO J. Appl. Phys. (1995), 78(3), 1944-7
CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English
AB The **band-gap** alignment of InAsI-xPx/In0.53Ga0.47As1-yPy strained heterostructures fabricated by selective As-P interdiffusion in an as-grown **InP**/In0.53Ga0.47As superlattice was studied using low-temp. photoluminescence. Interdiffusion is performed using thermal anneals with P gas ambient. By analyzing both the energy and the integrated intensity of the superlattice photoluminescence along with their dependences on excitation intensity, the superlattice band alignment is I for x < 0.58 and y < 0.21, whereas it switches to II for x < 0.58 and y > 0.21. Simulations show that in contrast to the type-I situation the band discontinuity mainly occurs in the conduction band for the type-II superlattice. The transition from type-I to type-II alignment is attributed to compn. changes and strain development at the heterointerfaces.

L67 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:287559 HCAPLUS
DN 120:287559
TI **Heterojunction** transistor
IN Fukano, Hideki
PA Nippon Telegraph & Telephone, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05326546	A2	19931210	JP 1992-148904	19920518

AB The transistor comprises a semiconductor substrate successively coated with a n-GauIn1-uPvAs1-v or AluGavIn1-u-vAs (0 .ltoreq. u .ltoreq. 1, 0 .ltoreq. v .ltoreq. 1) collector semiconductor layer, a 1st p-GaxIn1-xAsySb1-y (0 .ltoreq. x .ltoreq. 1, 0 .ltoreq. y .ltoreq. 1) base semiconductor layer, a 2nd p-GakIn1-kPlAs1-l (0 .ltoreq. k .ltoreq. 1, 0 .ltoreq. l .ltoreq. 1) or AlmGanIn1-m-nAs (0 .ltoreq. m .ltoreq. 1, 0 .ltoreq. n .ltoreq. 1) base semiconductor layer, and a n-GawIn1-wPzAs1-z or AlwGazIn1-w-zAs (0 .ltoreq. w .ltoreq. 1, 0 .ltoreq. z .ltoreq. 1) emitter semiconductor layer having an energy **band gap** wider than the 2nd base semiconductor layer. The transistor may comprise an **InP** substrate successively coated with a collector layer, a 1st base layer, a 2nd base layer, and an emitter layer, which have compns. lattice-commensurate with the substrate. The transistor has an improved withstand voltage.

> D BIB AB L69 1-41

L69 ANSWER 1 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:724021 HCAPLUS
DN 136:12409
TI Antimonide-based long-wavelength lasers on **GaAs** substrates
AU Klem, J. F.; Blum, O.
CS Sandia National Laboratories, Albuquerque, NM, 87185, USA
SO Proceedings - Electrochemical Society (2000), 2000-18(High Speed Compound Semiconductor Devices for Wireless Applications and State of the Art Program on Compound Semiconductors (XXXIII)), 82-90
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
AB The authors have studied the use of **GaAsSb** in edge-emitting laser active regions to obtain lasing near 1.3 .mu.m. Single quantum well **GaAsSb** devices display electroluminescence at wavelengths as long as 1.34 .mu.m, but substantial blue-shifts occur under high injection conditions. **GaAsSb** single quantum well edge emitters were obtained which lase at 1.275 .mu.m with a room-temp. threshold c.d. .gtoreq.535 A/cm2. Modification of the basic **GaAsSb/GaAs** structure with the addn. of **InGaAs** layers results in a strongly type-II band alignment which can be used to further extend the emission wavelength of these devices. Using **GaAsSb/InGaAs** active regions, lasers emitting at 1.17 .mu.m were obtained with room-temp. threshold current densities of 120 A/cm2, and devices operating at 1.29 .mu.m have displayed thresholds .gtoreq.375 A/cm2. Characteristic temps. for devices employing various **GaAsSb**-based active regions are 60-73K.
RE.CNT 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L69 ANSWER 2 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:596607 HCAPLUS
DN 135:296708
TI 300 GHz **InP/GaAsSb/InP** double **HBTs** with high current capability and BVCEO .gtoreq. 6 V
AU Dvorak, M. W.; Bolognesi, C. R.; Pitts, O. J.; Watkins, S. P.
CS Compound Semiconductor Device Laboratory, Simon Fraser University, Burnaby, BC, V5A 1S6, Can.
SO IEEE Electron Device Letters (2001), 22(8), 361-363
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB We report MOCVD-grown NpN **InP/GaAsSb/InP** abrupt double **heterojunction** bipolar transistors (DHBTs) with simultaneous values of fT and fMAX as high as 300 GHz for JC = 410 kA/cm2 at VCE = 1.8 V. The devices maintain outstanding dynamic performances over a wide range of biases including the satn. mode. In this material system the p+ **GaAsSb** base conduction band edge lies 0.10-0.15 eV above the **InP** collector conduction band, thus favoring the use of non-graded base-collector designs without the current blocking effect found in conventional **InP**/GaInAs-based DHBTs. The 2000 .ANG. **InP** collector provides good breakdown voltages of BVCEO = 6 V and a small collector signal delay of .apprx.0.23 ps. Thinner 1500 .ANG. collectors allow operation at still higher currents with fT > 200 GHz at JC = 650 kA/cm2.

RE.CNT 17 THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L69 ANSWER 3 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:545372 HCAPLUS
DN 135:130789
TI Compd. semiconductor epitaxial wafer for a **HBT**
IN Fujiu, Shinjiro; Otoki, Yohei; Saito, Toshiya
PA Hitachi Cable, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001203216	A2	20010727	JP 2000-13945	20000118

AB The invention relates to a semiconductor epitaxial wafer for **HBT** (**heterojunction** bipolar transistor), suited for use in mm-wave digital communication systems, wherein the **GaAs** base layer is sepd. from the GaInP emitter layer by any of InAs, **InGaAs**, **InAsP**, GaAsP, AlGaAs layers.

L69 ANSWER 4 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:410680 HCAPLUS
DN 135:26440
TI MOCVD growth and optical properties of **gallium arsenide** antimonide/**indium gallium arsenide** and **gallium arsenide** antimonide/**indium phosphide** heterostructures
AU Hu, Jinsheng
CS Simon Fraser Univ., Burnaby, BC, Can.
SO (1999) 117 pp. Avail.: UMI, Order No. DANQ51872
From: Diss. Abstr. Int., B 2001, 61(7), 3652
DT Dissertation
LA English
AB Unavailable

L69 ANSWER 5 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:2267 HCAPLUS
DN 134:155869
TI Deep-level defects at lattice-mismatched interfaces in **GaAs** -based **heterojunctions**
AU Wosinski, T.; Yastrubchak, O.; Makosa, A.; Figielski, T.
CS Institute of Physics, Polish Academy of Sciences, Warsaw, 02-668, Pol.
SO Journal of Physics: Condensed Matter (2000), 12(49), 10153-10160
CODEN: JCOMEL; ISSN: 0953-8984
PB Institute of Physics Publishing
DT Journal
LA English
AB Elec. properties of lattice mismatch-induced defects in **GaAs** /(Ga,As)Sb and **GaAs**/(In,Ga)As **heterojunctions** have been studied by means of an electron-beam-induced current in a SEM microscope and deep-level transient spectroscopy (DLTS). DLTS measurements, carried out with p-n junctions formed at the interfaces, revealed one electron trap and two hole traps induced by the lattice mismatch. The electron trap, at about Ec - 0.68 eV, is attributed to electron states assocd. with threading dislocations in the ternary compd. By comparing the concn. of this trap, revealed by DLTS, with EBIC results

on the diffusion length, obtained for **heterojunctions** with different lattice mismatches, it is inferred that the minority-carrier lifetime is controlled by dislocations in the epilayer region close to the interface. Two new hole traps are ascribed to defects assocd. with the lattice-mismatched interface of the heterostructures.

RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L69 ANSWER 6 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:551478 HCAPLUS
DN 133:142457
TI Semiconductor laser devices
IN Nishi, Kenichi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000223776	A2	20000811	JP 1999-19089	19990127
	JP 3230576	B2	20011119		

AB The devices, emitting the light vertically, comprise: an n-**GaAs** substrate; and an active layer comprising a quantum well layer (thickness < de Broglie wavelength; e.g. AlGaAs, GaInAs, **GaAsSb**) and a laminate having a quantum wire or a quantum dot structure (e.g. GaInAs).

L69 ANSWER 7 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:462457 HCAPLUS
DN 133:158246
TI In0.53Ga0.47As/GaAs1-xSbx type II strained MQW structures grown on **InP** by molecular beam epitaxy
AU Harada, H.; Kawamura, Y.; Katayama, T.; Takasaki, H.; Yamamoto, A.; Naito, H.; Inoue, N.
CS Research Institute for Advanced Science and Technology, Osaka Prefecture University, Osaka, 599-8570, Japan
SO Mem. Inst. Sci. Ind. Res., Osaka Univ. (2000), 57(Third SANKEN International Symposium, 2000), 291
CODEN: MISIAW; ISSN: 0369-0369
PB Osaka University, Institute of Scientific and Industrial Research
DT Journal
LA English
AB Type-II strained multiple quantum wells (MQW) were grown on Fe-doped (100) **InP** substrates at 505.degree. by solid-source MBE and were characterized by XRD and PL measurements. Samples with a lattice mismatch f = 0, 0.39, and 0.92% and MQW periods of 70, 20, and 10 periods were examd. At a lattice mismatch of f = 0.92, the crystal quality of the MQW layer was degraded which could be seen from the broadening of the full width at half max. (FWHM) of the XRD peaks and the missing of a PL signal. With decreasing MQW periods, the FWHM of the XRD peak of a sample with f = 0.92% became sharp and a PL signal was obsd. at 2.9 .mu.m which is much longer than that (2.2 .mu.m) of the lattice-matched MQW layers.

RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L69 ANSWER 8 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:91243 HCAPLUS
DN 132:173025

TI Optics of excitons in **InGaAs/InP** quantum wells
AU Borgulova, J.; Rheinlander, B.; Kovae, J.; Uherek, F.; Gottschalch, V.; Wagner, G.; Nassauer, S.; Benndorf, G.; Gerhardt, M.; Skriniarova, J.; Jakabovie, J.
CS Department of Microelectronics, Slovak University of Technology, Bratislava, 812 19, Slovakia
SO Int. Conf. Indium Phosphide Relat. Mater., 11th (1999), 515-518 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.
CODEN: 68QKA4
DT Conference
LA English
AB The authors report on the anal. of the structures with In0.53Ga0.47As/ **InP** quantum wells (QW) for the use in tunable resonant cavity enhanced photodetectors operating at the wavelength of 1550 nm. The structures were prepd. by low-pressure OMVPE. The optical properties were analyzed by spectral ellipsometry, photoluminescence and photocurrent measurements. The excitonic transition energies are slightly shifted to lower values in comparison with theor. model. This difference can be explained by the formation of InAs or **InAsP** monolayer at the interface between **InGaAs** QW and **InP** barrier. For the MQW pin diode with 20 wells the authors measured a Stark shift of 20 meV at an applied elec. field of 10 V/i.m.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L69 ANSWER 9 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:86586 HCAPLUS
DN 132:215272
TI Electrical stress damage reversal in non-passivated fully self-aligned **InP HBTs** by ozone surface treatment
AU Matine, N.; Soerensen, G.; Bolognesi, C. R.; DiSanto, D.; Xu, X.; Watkins, S. P.
CS School of Engineering Science, Compound Semiconductor Device Laboratory (CSDL), Simon Fraser University, BC, V5A 1S6, Can.
SO Electron. Lett. (1999), 35(25), 2229-2231
CODEN: ELLEAK; ISSN: 0013-5194
PB Institution of Electrical Engineers
DT Journal
LA English
AB The authors report that the degrdn. of device characteristics due to elec. stressing in non-passivated fully self-aligned **InP**-based heterostructure bipolar transistors (**HBTs**) can be reversed by a simple surface treatment in ozone. The technique is demonstrated on MOCVD-grown **InP**/GaAs0.51Sb0.49/**InP** double heterostructure bipolar transistors (DHBTs) with a C-doped base, and on conventional MBE-grown **InP**/Ga0.47In0.53As single heterostructure bipolar transistors (SHBTs) with a Be-doped base. This is the first report of the reversibility of bias stress damage in the extrinsic region of III-V **HBTs**: the expts. presented confirm that stress damage occurs at the exposed emitter periphery, thus explaining the success of emitter ledge passivation techniques.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L69 ANSWER 10 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:37581 HCAPLUS
DN 132:188160
TI Spin-dependent resonant tunneling in semiconductor nanostructures
AU De Andrada e Silva, Erasmo A.; La Rocca, Giuseppe C.

CS Instituto Nacional de Pesquisas Espaciais, Sao Jose dos Campos, 12201, Brazil
SO Braz. J. Phys. (1999), 29(4), 719-722
CODEN: BJPHE6; ISSN: 0103-9733
PB Sociedade Brasileira de Fisica
DT Journal
LA English
AB The spin-dependent quantum transport of electrons in non magnetic III-V semiconductor nanostructures was studied theor. within the envelope function approxn. and the Kane model for the bulk. An unpolarized beam of conducting electrons can be strongly polarized in zero magnetic field by resonant tunneling across asym. double-barrier structures, as an effect of the spin-orbit interaction. The electron transmission probability is calcd. as a function of energy and angle of incidence. Specific results for tunneling across lattice matched polytype Ga0.47In0.53As/ **InP** /Ga0.47In0.53As / GaAs0.5Sb0.5/ Ga0.47In0.53As double barrier heterostructures show sharp spin split resonances, corresponding to resonant tunneling through spin-orbit split quasi-bound electron states. The polarization of the transmitted beam is also calcd. and is over 50%.
RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L69 ANSWER 11 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:5390 HCAPLUS
DN 132:101079
TI Zinc diffusion in In(As,P)/(In,Ga)As heterostructures
AU Ettenberg, Martin H.; Lange, Michael J.; Sugg, Alan R.; Cohen, Marshall J.; Olsen, Gregory H.
CS Sensors Unlimited, Inc., Princeton, NJ, 08540, USA
SO J. Electron. Mater. (1999), 28(12), 1433-1439
CODEN: JECMA5; ISSN: 0361-5235
PB Minerals, Metals & Materials Society
DT Journal
LA English
AB A systematic study of the sealed ampul diffusion of zinc into epitaxially grown **InP**, In0.53Ga0.47As, In0.70Ga0.30As, In0.82Ga0.18As, and through the In(As,P)/(In,Ga)As interface is presented. Diffusion depths were measured using cleave-and-stain techniques, electrochem. profiling, and SIMS spectroscopy. The diffusion coeffs., D = D0e-Ea/kT, were derived. For **InP**, D0 = 4.82 .times. 10-2 cm2/s and Ea = 1.63 eV and for In0.53Ga0.47As, D0 = 2.02 .times. 104 cm2/s and Ea = 2.63 eV. Diffusion into the heteroepitaxial structures used in the fabrication of planar PIN photodiodes is dominated by the effects of the **InP** /(In,Ga)As interface.
RE.CNT 22 THERE ARE 22 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L69 ANSWER 12 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:716325 HCAPLUS
DN 131:316671
TI Semiconductor device and fabrication thereof
IN Shigematsu, Toshio; Imanishi, Kenji; Tanaka, Hitoshi
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1
PATENT NO. KIND DATE APPLICATION NO. DATE

PI JP 11312685	A2	19991109	JP 1998-118466	19980428
US 2002027232	A1	20020307	US 1998-191543	19981113
PRAI JP 1998-118466	A	19980428		

AB The invention relates to a semiconductor device, i.e., a **heterojunction** bipolar transistor, suited for use in optical communication systems, wherein the layout of base and base lead layers minimizes base resistance.

L69 ANSWER 13 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:384353 HCAPLUS
DN 131:137404
TI Electron-spin polarization by resonant tunneling
AU de Andrada e Silva, Erasmo A.; La Rocca, Giuseppe C.
CS Instituto Nacional de Pesquisas Espaciais, Sao Jose dos Campos, Sao Paulo, 12201, Brazil
SO Phys. Rev. B: Condens. Matter Mater. Phys. (1999), 59(24), R15583-R15585
CODEN: PRBMDO; ISSN: 0163-1829
PB American Physical Society
DT Journal
LA English
AB The spin-dependent electron resonant tunneling through nonmagnetic III-V semiconductor asym. double barriers was studied theor. within the envelope function approxn. and the Kane model for the bulk. It is shown, in particular, that an unpolarized beam of conducting electrons can be strongly polarized, at zero magnetic field, by a spin-dependent resonant tunneling, due to the Rashba mesoscopic spin-orbit interaction. The electron transmission probability is calcd. as a function of the electron's energy and angle of incidence. Specific results for tunneling across lattice matched polytype Ga0.47In0.53As/**InP** /Ga0.47In0.53As/GaAs0.5Sb0.5/Ga0.47In0.53As double barrier nanostructures show, for instance, sharp spin-split resonances, corresponding to resonant tunneling through spin-orbit split quasibound ground and excited electron states (quasisubbands). The calcd. polarization of the transmitted beam in resonance with the 2nd quasisubband shows that polarization bigger than 50% can be achieved with this effect.
RE.CNT 19 THERE ARE 19 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L69 ANSWER 14 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:288524 HCAPLUS
DN 131:37420
TI A new polarization-insensitive 1.55-.mu.m **InGaAs**(P)-InGaAsP multiquantum-well electroabsorption modulator using a strain-compensating layer
AU Chung, Ku-Ho; Shim, Jong-In
CS Department of Electronic Engineering, Hanyang University, Kyungki, 425-791, S. Korea
SO IEEE J. Quantum Electron. (1999), 35(5), 730-736
CODEN: IEJQA7; ISSN: 0018-9197
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB In a conventional polarization-insensitive multiquantum-well electroabsorption modulator, it is normal to apply tensile and compressive strain on the well and the barrier, resp. But the main disadvantages of such a structure are a low conduction band offset (0.04-0.06 eV), a high heavy-hole band offset (0.20-0.24 eV), and a relatively large well thickness (110-120 .ANG.). The authors propose a new method of overcoming

these disadvantages by placing a tensile strain on both the well and the barrier and compensating for them with a compressive strained intrinsic layer.

RE.CNT 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L69 ANSWER 15 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:131404 HCAPLUS
DN 130:344451
TI Luminescent characteristics of five component heterostructures based on AIIIBV compounds
AU Lozovskii, V. N.; Lunin, L. S.; Alfimova, D. L.
CS Novocherkassk. Gos. Tekh. Univ., Novocherkassk, Russia
SO Izv. Vyssh. Uchebn. Zaved., Sev.-Kavk. Reg., Estestv. Nauki (1997), (4), 47-50
CODEN: IVUNE6; ISSN: 1026-2237
PB Rostovskii Gosuniversitet
DT Journal
LA Russian
AB The Group IIIA-pnictide 5-component solid soln. epilayers were grown from the liq. phase by the temp. gradient zone recrystn. method. The photoluminescence of Group IIIA-pnictide 5-component heterostructures was studied.

L69 ANSWER 16 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:698224 HCAPLUS
DN 130:44766
TI Type II photoluminescence and conduction band offsets of **GaAsSb/InGaAs** and **GaAsSb/InP** heterostructures grown by metalorganic vapor phase epitaxy
AU Hu, J.; Xu, X. G.; Stotz, J. A. H.; Watkins, S. P.; Curzon, A. E.; Thewalt, M. L. W.; Matine, N.; Bolognesi, C. R.
CS Department of Physics, Simon Fraser University, Burnaby, BC, V5A 1S6, Can.
SO Appl. Phys. Lett. (1998), 73(19), 2799-2801
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB The optical properties of lattice-matched **GaAsSb/InGaAs/InP** heterostructures with a varying **InGaAs** layer thickness (0-900 .ANG.) were studied. These structures display strong low temp. type II luminescence, the energy of which varies with the **InGaAs** layer thickness and ranges from 0.453 to 0.63 eV. The type II luminescence was used to det. directly and accurately the conduction band offset of these structures. The values obtained herein are 0.36 and 0.18 eV at 4.2 K for the **GaAsSb/InGaAs** and **GaAsSb/InP heterojunctions**, resp., with the **GaAsSb** conduction band higher in energy.

RE.CNT 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L69 ANSWER 17 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:562629 HCAPLUS
DN 129:252210
TI Efficient modeling of the optical properties of MQW modulators on InGaAsP with absorption edge merging
AU Ashland, Andreas; Schulz, Dirk; Voges, Edgar
CS Univ. of Dortmund, Dortmund, D-44221, Germany
SO IEEE J. Quantum Electron. (1998), 34(9), 1597-1603

CODEN: IEJQA7; ISSN: 0018-9197
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB The optical properties of quantum wells on GaxIn1-x As1-yPy are studied. The dielec. function .epsilon.(.omega.) is calcd. with a d. matrix formalism valid for excitonic transitions as well as for the interband absorption including band mixing. With 2 simple approxns., the required no. of overlap integrals is greatly reduced, allowing a fast and efficient exciton calcn. The calcn. results are compared with measurements at 77 K and at a room temp. of 300 K. Also, the authors present a field-induced heavy and light hole absorption merging for a Ga.epsilon.In1-xAs1-yPy-based modulator for the 1st time. It can be operated at a wavelength .lambda. = 1.55 .mu.m, showing a very large absorption change and a small neg. chirp factor, which is recommended for a low bit error rate.

L69 ANSWER 18 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:426400 HCAPLUS
DN 129:167862
TI Band offsets in near-**GaAs** alloys
AU Whitaker, M. F.; Dunstan, D. J.; Hopkinson, M.
CS Department of Physics, Queen Mary and Westfield College, University of London, London, E1 4NS, UK
SO Inst. Phys. Conf. Ser. (1998), 156(Compound Semiconductors 1997), 279-282
CODEN: IPCSEP; ISSN: 0951-3248
PB Institute of Physics Publishing
DT Journal
LA English
AB The authors det. the band offset ratio of **GaAs**/GaXAs heterostructures, where X is any alloying element (e.g. In, Al, P, Sb), by studying GaXAs/AlGaAs superlattices. Photoluminescence is measured at both ambient and high pressure from **GaAs** and GaXAs quantum wells and this yields the band offset ratio of the GaXAs/**GaAs** interface. To confirm the technique, the band offset ratio of **GaAs**/AlGaAs is detd. in this paper using this general method, and the result agrees well with previously published data obtained more directly.

L69 ANSWER 19 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:54104 HCAPLUS
DN 128:173855
TI Electroabsorption multiple quantum well modulators for high frequency applications
AU Chang, W. S. C.; Loi, K. K.; Liao, H. H.; Hodiak, J.; Yu, P. K. L.; Asbeck, P. M.
CS Department of Electrical and Computer Engineering, University of California, La Jolla, CA, 92093-0407, USA
SO Proc. SPIE-Int. Soc. Opt. Eng. (1997), 3290(Optoelectronic Integrated Circuits II), 142-156
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering
DT Journal
LA English
AB External modulation of continuous-wave laser radiation by multiple quantum well electroabsorption modulators will potentially play an important role in RF photonic links, esp. at high microwave frequencies and millimeter waves. **InAsP**/GaInP MQW on **InP** and GaInAs/InAlAs MQW on **GaAs** modulators were grown by MBE and fabricated into p-i-n modulators. Performance with -26 dB link efficiency without

amplification, 5 dB insertion loss, 15 mW of optical power and 17 GHz bandwidth was exptl. demonstrated. Extension to 100 GHz bandwidth with -39 dB link efficiency (without amplification) can be expected. Traveling wave modulators and on-chip impedance matching of p-i-n modulators were designed, fabricated and evaluated. Traveling wave modulators with flat frequency response over 40 GHz were exptl. demonstrated.

L69 ANSWER 20 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:361444 HCAPLUS
DN 126:336619
TI Semiconductor heterostructure radiation detector having two sensitivity ranges
IN Schneider, Harald; Schoenbein, Clemens
PA Fraunhofer-Gesellschaft zur Foerderung der Angewandten Forschung e.V., Germany
SO Ger. Offen., 7 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19538650	A1	19970424	DE 1995-19538650	19951017
	DE 19538650	C2	19970828		
	WO 9717719	A2	19970515	WO 1996-DE1983	19961016
	WO 9717719	A3	19970703		
	W: CA, US				
	RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	EP 856201	A2	19980805	EP 1996-945510	19961016
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI				
	US 6130466	A	20001010	US 1998-61282	19980417
PRAI	DE 1995-19538650	A	19951017		
	WO 1996-DE1983	W	19961016		

AB A heterostructure radiation detector is described, having 2 adjacent semiconductor layer regions sensitive in different spectral ranges, in which photons with different energies are absorbed which optically excite the charge carriers present in the semiconductor layer regions such that a photocurrent can be generated in the corresponding semiconductor layer region which depends on the external elec. potential applied to the electrodes of the device. One semiconductor layer region is a photodiode and the other is a quantum well intersubband photodetector.

L69 ANSWER 21 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:249671 HCAPLUS
DN 126:323930
TI p-Channel, ion implanted, **GaAsSb**/InAlAs HIGFETs on **InP** for digital and microwave applications
AU Cerny, C. L. A.; Merkel, K. G.; Schuermeyer, F. L.; Bright, V. M.; Kaspi, R.
CS Solid State Electronics Directorate, Wright Laboratory, WPAFB, OH, 45433-7319, USA
SO Proc. - IEEE/Cornell Conf. Adv. Concepts High Speed Semicond. Devices Circuits (1995) 253-259
CODEN: PIDCEA; ISSN: 1079-4700
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB The authors report the 1st device results of ion implanted, recessed gate,

p-channel **GaAsSb**/InAlAs HIGFETs grown lattice matched to **InP** with tremendous potential for use in a complementary technol. on III-V substrates. The InAiAs/**GaAsSb** heterostructure possesses excellent hole confinement, and this is coupled to a p-channel device process which employs ion implanted contacts and a recessed gate. This implies the **GaAsSb**/InAlAs p-channel HIGFET has advantages in both digital and microwave design. Close examn. of the **GaAsSb** /InAlAs heterostructure material during process development, provides an important feedback loop which resulted improved p-channel device characteristics. Microstructural evaluation of the ohmic contacts and its effect on their elec. stability are presented. D.c. characteristics and unique photoelec. characterization results on the fabricated p-channel HIGFETs are provided. Comments on maturing **GaAsSb**/InAlAs HIGFETs into a self-aligned gate, submicron, complementary technol. for integrated circuit applications will be outlined.

L69 ANSWER 22 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:700002 HCAPLUS
DN 126:122935
TI Interface abruptness in strained III-V heterostructures
AU Bruni, M. R.; Kaciulis, S.; Mattogno, G.; Righini, G.
CS Istituto di Chimica dei Materiali, CNR, P.O. Box 10, Monterotondo Scalo, I-00016, Italy
SO Appl. Surf. Sci. (1996), 104/105(Proceedings of the Fifth International Conference on the Formation of Semiconductor Interfaces, 1995), 652-655
CODEN: ASUSEE; ISSN: 0169-4332
PB Elsevier
DT Journal
LA English
AB Highly strained In0.53Ga0.47As/InAs/In0.53Ga 0.47As heterostructures and InAs layers were grown on **InP**(100) substrates by using mol. beam epitaxy (MBE). The samples have been investigated by means of selected-area X-ray spectroscopy (SAXPS) combined with low energy ion sputtering. The heterointerface widths in the In0.53Ga0.47As/InAs/In0.53Ga0.47As samples grown under diverse MBE conditions (std. and virtual surfactant) have been analyzed. The thickness of the ternary sublayer formed between the InAs and **InP** substrate has been studied in the samples deoxidized under the flux of arsenic (AsH3) or phosphorus (PH3). The suitability of SAXPS depth profiling technique for the qual. characterization of ultra-thin heterostructures is discussed considering the limitations of exptl. depth resoln.

L69 ANSWER 23 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:676959 HCAPLUS
DN 125:344192
TI Determination of the thermal properties of semiconductors using the photothermal method in the many thin layers case
AU Saadallah, F.; Yacoubi, N.; Hfaiedh, A.
CS I.P.E.I.N., Merazka, 8000, Tunisia
SO Opt. Mater. (Amsterdam) (1996), 6(1/2), 35-39
CODEN: OMATET; ISSN: 0925-3467
DT Journal
LA English
AB The photothermal method has been used in order to det. the thermal properties of semiconductors. In this work, a simple expression for the periodic temp., at the sample's surface, which is valuable for a no. of layers deposited on a substrate, was introduced. This expression showed a very good agreement with data obtained using the **GaAsSb**/

GaAs and **InP**/GaInAs/**InP** heterostructures, when the sum of the thicknesses of all the layers is much smaller than the thickness of the substrate. This condition is often satisfied when dealing with semiconductors used in microoptoelectronics.

L69 ANSWER 24 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:484052 HCAPLUS
DN 125:260391
TI Optimized second-harmonic generation in asymmetric double quantum wells
AU Vurgaftman, Igor; Meyer, Jerry R.; Ram-Mohan, L. Randas
CS National Res. Council-NRL Res. Associateship, Washington, DC, 20375, USA
SO IEEE J. Quantum Electron. (1996), 32(8), 1334-1346
CODEN: IEJQA7; ISSN: 0018-9197
DT Journal
LA English
AB The authors present a theor. anal. of surface-incidence and waveguide-mode 2nd harmonic generation with detuned intersubband transitions in **GaAs**-AlGaAs, **InGaAs**-InAlAs and GaSb-**InGaSb**-AlGaSb asym. double quantum wells. The anal. includes the effects of absorption, satn., pump depletion, optical carrier heating, mode confinement and competition, and the loss of phase coherence due to waveguide, bulk and resonant intersubband contributions to the refractive index mismatch. Optimal structure were detd. for each material system in both surface-incidence and waveguide-mode geometries. A scheme for maintaining phase matching by incorporation of a sep. region with an intersubband transition tuned midway between the 1st and 2nd harmonic frequencies is analyzed. At 10.6 .mu.m, the max. conversion efficiency for the optimized **InGaAs**-InAlAs waveguide-mode device is .apprxeq. 16% at a pump-beam intensity of 40 MW/cm2. Also, the same device can be modulated to vanishing 2nd harmonic output power when an elec. field of -32 kV/cm is applied.

L69 ANSWER 25 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:245262 HCAPLUS
DN 124:321458
TI **GaAsSb**-based **heterojunction** tunnel diodes for tandem solar cell interconnects
AU Zolper, John C.; Klem, John F.; Plut, Thomas A.; Tigges, Chris P.
CS Sandia National Laboratories, Albuquerque, NM, 87185-0603, USA
SO Conf. Rec. IEEE Photovoltaic Spec. Conf. (1994), 24th(1994 IEEE First World Conference on Photovoltaic Energy Conversion, Vol. 2), 1843-6
CODEN: CRCNDP; ISSN: 0160-8371
DT Journal
LA English
AB We report a new approach to tunnel junctions that employs a pseudomorphic **GaAsSb** layer to obtain a band alignment at an **InGaAs** or InAlAs p-n junction favorable for forward bias tunneling. Since the majority of the band offset between **GaAsSb** and **InGaAs** or InAlAs is in the valence band, when a **GaAsSb** layer is placed at an **InGaAs** or InAlAs p-n junction the tunneling distance is reduced and the tunneling current is increased. For all doping levels studied, the presence of the **GaAsSb**-layer enhanced the forward tunneling characteristics. In fact, in an **InGaAs/GaAsSb** tunnel diode with p = 1.5.times.1018 cm-3 a peak tunneling current sufficient for a 1000 sun **InP/InGaAs** tandem solar cell interconnect was achieved while a similarly doped all-**InGaAs** diode was rectifying. This approach affords a new degree of freedom in designing tunnel junctions for tandem solar cell interconnects. Previously only doping levels could be varied to control the tunneling

properties. Our approach relaxes the doping requirements by employing a **GaAsSb**-based **heterojunction**.

L69 ANSWER 26 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:178958 HCAPLUS
DN 124:247991
TI **Hetero-junction** bipolar transistor
IN Kurishima, Kenji; Kobayashi, Takashi
PA Nippon Telegraph & Telephone, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07326629	A2	19951212	JP 1994-142212	19940602

AB The transistor, comprising a collector layer of **InGaAs** or **InP** on an **InP** substrate, a base layer of **InGaAs** on it, and an emitter layer of InGaAsP or InAlGaAs, contains a spacer layer of **InAsP** where its electron energy at the end of valence-electron band is lower than that of the base layer, between the collector and the base layer. The transistor may have a sub-spacer layer of **InGaAs** with higher dopant concn. than that of the collector layer. The spacer layer may be distorted superlattice of InAs-**InP**, where the electron energy at the end of valence-electron band is lower than that of the base layer. The spacer layer may have a compn. gradient of As in the film-thickness direction decreasing continuously toward the collector-layer side. In the distorted superlattice, the film thickness of the InAs layer may decrease toward the collector-layer side, and that of the **InP** layer may increase in the same direction. The transistor prevents hole leak from the collector layer to the base layer to give an improved **HBT** resistant for high-speed operation.

L69 ANSWER 27 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:621545 HCAPLUS
DN 123:23802
TI Semiconductor devices and manufacture thereof
IN Mochizuki, Kazuhiro; Tagami, Tomonori; Masuda, Hiroshi; Horiuchi, Katsutada; Mishima, Tomoyoshi; Nakamura, Tooru
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 34 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06252163	A2	19940909	JP 1993-276484	19931105
PRAI	JP 1992-347688		19921228		

AB The device has a polycryst. conductive layer from a compd. semiconductor (e.g., Group IIIA pnictide, and/or doped with Be or C) .ltoreq.0.04 .OMEGA.cm in resistivity. The device may be a **heterojunction** bipolar transistor, surface-emitting laser, or a **heterojunction** insulated gate FET. The title process comprises formation of a 1st film (e.g., insulating film) on a substrate, and formation of the polycryst. Group IIIA pnictide layer .ltoreq.0.04 .OMEGA.cm in resistivity at .ltoreq.550.degree. in substrate temp. by MBE, metalorg. VPE, or metalorg. MBE at .gtoreq.20 in pnicogen/Group IIIA element ratio. Use of the

polycryst. conductive layer for the base draw-out layer lowers base-collector parasite capacitance without increase of base resistance, and a complete current constriction structure is formed by connection of the device intrinsic and the device parasite region to the polycryst. conductive layer for a laser.

L69 ANSWER 28 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:424832 HCAPLUS
DN 121:24832
TI Semimetal-semiconductor heterostructures and multilayers
IN Golding, Terry D.; Miller, John H., Jr.
PA University of Houston, USA
SO PCT Int. Appl., 29 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9402665	A1	19940203	WO 1993-US6955	19930719
	W: CA, JP				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 5449561	A	19950912	US 1992-916050	19920717
	EP 649480	A1	19950426	EP 1993-917329	19930719
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LI, LU, MC, NL, PT, SE				
	JP 08501901	T2	19960227	JP 1993-504725	19930719
	US 5686351	A	19971111	US 1995-447477	19950523
PRAI	US 1992-916050		19920717		
	WO 1993-US6955		19930719		

AB The present invention provides for the fabrication of single-layer semimetal/semiconductor heterostructures and multilayer semimetal/semiconductor structures. Each semimetal/semiconductor layer fabricated in accordance with the present invention has compatible crystal symmetry across the **heterojunction** between a semimetal and a semiconductor. A single-layer semimetal/semiconductor structure is fabricated by growing a rhombohedral semimetal in a [111] direction on a substrate material having a (111) orientation, and then growing a zinc blende semiconductor in a [111] direction on the semimetal. A multilayer semimetal/semiconductor structure may be grown from the single-layer semimetal/semiconductor structure by growing an addnl. rhombohedral semimetal layer in a [111] direction on the preceding semiconductor grown, then growing an addnl. zinc blende semiconductor layer in a [111] direction on the addnl. semimetal layer, and then repeating this process as many times as desired. Each semimetal to be sandwiched between semiconductors in the multilayer semimetal/semiconductor structure may be grown thin enough that the semimetal is converted into a semiconductor.

L69 ANSWER 29 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:122721 HCAPLUS
DN 120:122721
TI NPN **heterojunction** bipolar transistor including an antimonide base formed on a semi-insulating **indium phosphide** substrate
IN Stanchina, William E.; Hasenberg, Thomas C.
PA Hughes Aircraft Co., USA
SO Eur. Pat. Appl., 7 pp.
CODEN: EPXXDW
DT Patent
LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 571994	A2	19931201	EP 1993-108534	19930527
	EP 571994	A3	19940727		
	R: DE, FR, IT				
	US 5349201	A	19940920	US 1992-889864	19920528
	JP 06037104	A2	19940210	JP 1993-127404	19930528
	JP 2528253	B2	19960828		
PRAI	US 1992-889864		19920528		

AB A **heterojunction** bipolar transistor includes an **InGaAs**, **InP**, or AlInAs collector layer formed over an **InP** substrate. A base layer including Ga, As, and **Sb** is formed over the collector layer, and an AlInAs or **InP** emitter layer is formed over the base layer. The base layer may be ternary **GaAsSb** doped with Be.

L69 ANSWER 30 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:615522 HCAPLUS
DN 119:215522
TI Thermally stable **heterojunction** bipolar transistor
IN Iwata, Naotaka
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05090283	A2	19930409	JP 1991-251236	19910930

AB The title transistor comprises: an i- or n-type AlGaInAs layer approx. lattice-matched to **InP**; an i- or n-type **InP** layer; and a p-type AlGaAsSb layer, approx. lattice-matched to **InP**, formed between the 2 layers.

L69 ANSWER 31 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:663024 HCAPLUS
DN 117:263024
TI Semiconductor device
IN Inada, Tsuguo; Muto, Shunichi
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04118972	A2	19920420	JP 1990-237111	19900910
	JP 3000476	B2	20000117		
	US 5266814	A	19931130	US 1991-757185	19910910
PRAI	JP 1990-237111	A	19900910		

AB A semiconductor device having a resonant tunneling barrier structure and no base electrode is described, including a **heterojunction** structure having a light-incident window for generating an internal field in the barrier structure to control the tunneling current.

L69 ANSWER 32 OF 41 HCAPLUS COPYRIGHT 2002 ACS

AN 1992:643904 HCAPLUS
DN 117:243904
TI Semiconductor FET devices and manufacture thereof
IN Tagami, Tomonori; Hiruma, Takeyuki
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04127533	A2	19920428	JP 1990-247125	19900919

AB A strained-layer **heterojunction** device comprises: (1) a substrate, (2) a channel, (3) a buffer, (4) a cap, and (5) an undoped layer, wherein (2) and (3) are lattice-mismatched and -matched, resp., with (1); (2) is thinner than the dislocation-inducing crit. thickness; the source and the drain employ (1)-(4); and the gate employs (1), (2) and (5). The device is suited for use in high-speed LSI.

L69 ANSWER 33 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:559853 HCAPLUS
DN 117:159853
TI Photoluminescence of strained-layer quantum-well structures under high hydrostatic pressure
AU Wilkinson, W. A.
CS Univ. Surrey, Guildford/Surrey, GU2 5XH, UK
SO NATO ASI Ser., Ser. B (1991), 286(Front. High-Pressure Res.), 295-315
CODEN: NABPDS; ISSN: 0258-1221
DT Journal
LA English
AB The photoluminescence of quantum-well structures, under high hydrostatic pressure, was studied. An argon-loaded miniature diamond-anvil cell, which readily generates pressures in the region 0 to 200 kbar, was employed for this purpose. Structures contg. strained layers are currently of great interest and are concd. on here. High pressure techniques for detg. the **heterojunction** band line-ups, with spectroscopic accuracy, are described. Recent results on the **InGaAs**/AlGaAs and **GaAsSb/GaAs** strained systems are discussed. The pressure coeffs. of bulk semiconductors and more recently of low dimensional structures have been reported in the literature. There is now considerable evidence that compressively strained layers exhibit pressure coeffs. which are lower than expected. The influence of higher-order elastic contents and strain-dependent deformation potentials have been considered but do not adequately describe the data. This behavior therefore remains anomalous.

L69 ANSWER 34 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:201835 HCAPLUS
DN 116:201835
TI Interfacial properties of very thin gallium **indium** arsenide/ **indium phosphide** quantum well structures grown by metalorganic vapor phase epitaxy
AU Streubel, K.; Haerle, V.; Scholz, F.; Bode, M.; Grundmann, M.
CS 4. Phys. Inst., Univ. Stuttgart, Stuttgart, D-7000/80, Germany
SO J. Appl. Phys. (1992), 71(7), 3300-6
CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English

AB GaInAs/**InP** single quantum well structures with thicknesses <5 nm were grown by metal-org. vapor phase epitaxy at reduced pressure. The sharpness of the **heterojunctions** in this III/V system strongly depends on the applied gas switching sequence between the growth of the 2 materials caused by As carry-over after GaInAs and by Group VA atom exchange at the surface during a hydride stabilized growth interruption. The photoluminescence properties can be improved by adding intermediate monolayers of **InAsP** between **InP** and GaInAs and GaInAsP between GaInAs and **InP**. The photoluminescence of very thin quantum wells is split into multiplets due to the formation of growth islands at the interface. The size and lateral distribution of these islands were obsd. directly by cathodoluminescence anal. On the other hand, TEM measurements show that the interfaces within the growth island regions are not atomically smooth but of a certain roughness. Small microislands with diams. of a few lattice consts. form the "internal" interface structure.

L69 ANSWER 35 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:572662 HCAPLUS
DN 115:172662
TI Semiconductor crystal with heat-resistant **heterojunction**
IN Iwata, Naotaka
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 03038876	A2	19910219	JP 1989-172906	19890706
	JP 2576232	B2	19970129		

AB The crystal contains .gtoreq.1 AlAsxSb1-x or GaAsySb1-y layers between an InaAlbGa1-a-bAs layer and an IncAldGa1-c-dAs layer. The crystal may contain .gtoreq.1 InaAlbGa1-a-bAs layer between an AlAsxSb1-x layer and a GaAsySb1-y layer . The crystal is used in **heterojunction** diodes, FETs, bipolar transistors, etc. The crystal had heat-resistant **heterojunction**.

L69 ANSWER 36 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:154406 HCAPLUS
DN 114:154406
TI Preparation of heterostructure compound semiconductor devices by molecular beam epitaxy
IN Nakada, Yoshiaki
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 02240915	A2	19900925	JP 1989-60808	19890315
	JP 2528179	B2	19960828		

AB The title method uses a no. of beam sources of pnicogens each of which is adjusted to an optimum intensity corresponding to each of Group IIIA pnictide layers for sequential formation of the layers with shutter operation is in concordance with formation of **heterojunctions**.

Thus, using 2 As sources, an (In,Ga)As-Ga(As,Sb)-(In,Ga)As heterostructure was prepd.

L69 ANSWER 37 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:148641 HCAPLUS
DN 112:148641
TI Room-temperature **indium gallium arsenide** (**InGaAs**) detector arrays for 2.5 .mu.m
AU Olsen, G. H.; Joshi, A. M.; Mason, S. M.; Woodruff, K. M.; Mykietyn, E.; Ban, V. S.; Lange, M. J.; Hladky, J.; Erickson, G. C.; Gasparian, G. A.
CS Epitaxy, Inc., Princeton, NJ, 08540, USA
SO Proc. SPIE-Int. Soc. Opt. Eng. (1989), 1157(Infrared Technol. 15), 276-82
CODEN: PSISDG; ISSN: 0277-786X
DT Journal
LA English
AB New alloy **heterojunction** detectors of In0.8Ga0.2As/InAs0.6P0.4 are described which can detect light of 1.7-2.6 .mu.m with 50% quantum efficiency and 5 mA/cm2 dark current (-1V) d. at room temp. Wafer probe data showed that >50 good contiguous 100 .mu.m diam. devices (spaced 400 .mu.m) could be made on a 25 .times. 30 mm wafer with overall yield > 93%. The ability to operate under -1 V reverse bias makes these devices compatible with existing com. multiplexer readouts.

L69 ANSWER 38 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:128526 HCAPLUS
DN 112:128526
TI **Indium gallium arsenide/indium** arsenide phosphide antimonide diode lasers with output wavelengths at 2.52 .mu.m
AU Martinelli, Ramon U.; Zamerowski, Thomas J.
CS David Sarnoff Res. Cent., Princeton, NJ, 08450, USA
SO Appl. Phys. Lett. (1990), 56(2), 125-7
CODEN: APPLAB; ISSN: 0003-6951
DT Journal
LA English
AB **InGaAs**/InAsPSb double **heterojunction** oxide stripe lasers were grown by hydride vapor phase epitaxy. At 80 K, the threshold c.d. is 0.4 kA/cm2, the satd. output power is about 4 mW, and the differential quantum efficiency just above threshold is 20% per facet. The output wavelength increases from 2.44 .mu.m at 80 K to 2.52 .mu.m at 190 K. A layer of compositionally graded **InGaAs** accommodates the 2% lattice mismatch between the **InP** substrate and the laser structure. The operating characteristics of these lasers were compared with those of **InGaAs/InAsP** lasers. Their improved performance results from the better elec. and optical confinement of the InAsPSb cladding layers.

L69 ANSWER 39 OF 41 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:46926 HCAPLUS
DN 112:46926
TI High mobility transistor with opposed gates
IN Hollis, Mark A.; Goodhue, William D.; Nichols, Kirby B.; Bergeron, Normand, J., Jr.
PA Massachusetts Institute of Technology, USA
SO PCT Int. Appl., 43 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1